V

FILE NO. SRG/2019/002236

SCIENCE & ENGINEERING RESEARCH BOARD(SERB)

(A statutory body of the Department of Science & Technology, Government of India)

5 & 5A, Lower Ground Floor
Vasant Square Mall
Plot No. A, Community Centre
Sector-B, Pocket-5, Vasant Kunj
New Delhi-110070

Dated: 26-Nov-2019

ORDER

Subject: Financial Sanction of the research project titled **"Optimization of low cost lab-on-chip platforms for the development of biomedical applications"** under the guidance of Dr. Matta Durga Prakash, Electronics and Communication Engineering, Velagapudi Ramakrishna Siddhartha Engineering College , Kanuru, Vijayawada, Andhra pradesh-520007 - Release of 1st grant.

Sanction of **Science and Engineering Research Board (SERB)** is hereby accorded to the above mentioned project at a total cost of **Rs. 2344180/- (Rs.** Twenty Three Lakh Forty Four Thousand One Hundred and Eighty **Only)** with break-up of **Rs. *1097080/-* under Capital (Non-recurring) head** and **Rs.*1247100/-* under General (Recurring) head** for a duration of 24 months. The items of expenditure for which the total allocation of **Rs. 2344180/-** has been approved are given below:

S. No	Head	Total (in Rs.)
A	**Non-recurring**	
1	Equipment -> Electrochemical Analyzer -> Sol-Gel Deposition Equipment	1097080
A'	*Total (Non-Recurring)*	***1097080***
B	**Recurring Items**	
1	Recurring - I : (Manpower) Recurring - II : (Consumables, Travel, Contingencies, Other Cost) Recurring - III : Scientific Social Responsibility	744000 280000 10000
2	Recurring - IV : (Overhead Charges)	213100
B'	*Total (Recurring)*	***1247100***
C	**Total cost of the project (A' + B')**	**2344180**

2. Sanction of the **SERB** is also accorded to the payment of **Rs. 1097080/-** (Rupees Ten Lakh Ninety Seven Thousand and Eighty only) under 'Grants for creation of capital assets' and **Rs. 656050/-** (Rupees Six Lakh Fifty Six Thousand and Fifty only) under 'Grants-in-aid General' to **PRINCIPAL, Velagapudi Ramakrishna Siddhartha Engineering College , Kanuru** being the first installment of the grant for the year 2019-2020 for implementation of the said research project.

3. The expenditure involved is debitable to **Fund for Science & Engineering Research (FSER)**
This release is being made under Start-up Research Grant. (EC Engineering Sciences)

4. The Sanction has been issued to Velagapudi Ramakrishna Siddhartha Engineering College , Kanuru with the approval of the competent authority under delegated powers on **20 November, 2019** and vide Diary No. **SERB/F/6920/2019-2020** dated **21 November, 2019**

5. Sanction of the grant is subject to the conditions as detailed in Terms & Conditions available at website (www.serb.gov.in).

6. Overhead expenses are meant for the host Institute towards the cost for providing infrastructural facilities and general administrative support etc. including benefits to the staff employed in the project.

7. While providing operational flexibility among various subheads under head Recurring-II, it should be ensured that not more than Rs. 1 lakh each should be spent for travel and contingency.

8. Budget sanctioned under Scientific Social Responsibility (SSR) is meant only for activites enlisted under SSR norms and under no circumstances it can be reappropriated.

9. As per rule 211 of GFR, the accounts of project shall be open to inspection by sanctioning authority/audit whenever the institute is called upon to do so.

10. The sanctioned equipment would be procured as per GFR and its disposal of the same would be done with prior approval of SERB.

11. The release amount of **Rs. 1753130/-** (Rupees Seventeen Lakh Fifty Three Thousand One Hundred and Thirty only) will be drawn by the Under Secretary of the SERB and will be disbursed by means of RTGS transaction as per their Bank details given below:

PFMS Unique Code	**VRSEC**

Account Name	**V.R.SIDDHARTHA ENGINEERING COLLEGE**
Account Number	**33672200004978**
Bank Name & Branch	**SYNDICATE BANK VRSEC CMAPUS, KANURUVRSEC CAMPUS, KANURU, VIJAYAWADA-520007**
IFSC/RTGS Code	**SYNB0003367**
Email id of A/C Holder	**principal@vrsiddhartha.ac.in**
Email id of PI	**mdprakash82@gmail.com**

12.The institute will furnish to the SERB, separate Utilization certificate(UCs) financial year wise to the SERB for Recurring (Grants-in-aid General) & Non-Recurring (Grants for creation of capital assets) and an audited statement of accounts pertaining to the grant immediately after the end of each financial year.

13. The institute will maintain separate audited accounts for the project. A part or whole of the grant must be kept in an interest earning bank account which is to be reported to SERB. The interest thus earned will be treated as credit to the institute to be adjusted towards further installment of the grant.

14. The project File no. SRG/2019/002236 may also be mentioned in all research communications arising from the above project with due acknowledgement of SERB.

15. The manpower sanctioned in the project, if any is co-terminus with the duration of the project and SERB will have no liability to meet the fellowship and salary of supporting staff if any. beyond the duration of the project

16. As this is the first grant being released for the project, no previous U/C is required.

17. The institute may refund any unspent balance to SERB by means of a Demand Draft favoring "FUND FOR SCIENCE AND ENGINEERING RESEARCH" payable at New Delhi.

18. The organization/institute/university should ensure that the technical support/financial assistance provided to them by the Science & Engineering Research Board should invariably be highlighted/ acknowledged in their media releases as well as in bold letters in the opening paragraphs of their Annual Report.

19. In addition, the investigator/host institute must also acknowledge the support provided to them in all publications, patents and any other output emanating out of the project/program funded by the Science & Engineering Research Board.

(Dr. Ramesh Vijayan)
SCIENTIST-C
drvramesh@serb.gov.in

To,
Under Secretary
SERB, New Delhi
Copy forwarded for information and necessary action to: -

1.	The Principal Director of Audit, A.G.C.R.Building, IIIrd Floor I.P. Estate, Delhi-110002
2.	Sanction Folder, SERB , New Delhi.
3.	File Copy
4.	**Dr. Matta Durga Prakash** **Electronics and Communication Engineering** **Velagapudi Ramakrishna Siddhartha Engineering College , Kanuru, Vijayawada, Andhra pradesh-520007** **Email: mdprakash82@gmail.com** **Mobile: 919493595814** (Start date of the project may be intimated by name to the undersigned. For guidance, terms & Conditions etc. Please visit www.serb.gov.in.)
5.	**PRINCIPAL,** **Velagapudi Ramakrishna Siddhartha Engineering College , Kanuru** (Receipt of Grant may be intimated by name to the undersigned)

(Dr. Ramesh Vijayan)
SCIENTIST-C
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Optimization of low cost lab-on-chip platforms for the development of biomedical applications

File Number : SRG/2019/002236

Submitted By :

Dr. Matta Durga Prakash Submission

Date : 03-May-2019

PROPOSAL DETAILS

(SRG/2019/002236)

Dr. Matta Durga Prakash

mdprakash82@gmail.com
Associate Professor (Electronics and Communication Engineering)

Velagapudi Ramakrishna Siddhartha Engineering College

Kanuru, Vijayawada, Andhra pradesh-520007

Technical Details :

Lab-on-Chip technology implies those techniques that perform various laboratory operations on a miniaturized scale such as chemical synthesis and analysis on a single chip leading to a handheld and portable device. In other words, LoC is a device that is capable of scaling the single or multiple laboratory functions down to chip-format. The size of this chip ranges from millimeters to a few square centimeters. LoC is basically the integration of fluidics, electronics, optics and biosensors. The main motive of LoC is the need for the state-of-art pathological analysis on-the-go. LoCs prove to be useful for finding the methods for the early stage diagnosis of deadly and chronic diseases. Due to the advent of advanced technologies such as MEMS, NEMS, the integration of large number of interdisciplinary modules on a single chip. The various steps involved in Lab- on-Chip processing. The LoC processing initiates by collecting the physiological sample and then from this sample, the extraction of particular analyte/biomarker is done. Depending upon the biomedical application, the transducer will act on the analyte electrically, electromechanically optically or mechanically. The next step involves counting, sorting and amplification of the transducer output is performed according to the application. Finally, the amplified sample is processed using microelectronics techniques. Current trend shows the growth of research in this area. In many universities across the world, many groups are formed that are dedicating their research in this area. For example, BIOS in University of Twente, Mina Med in Germany, and Nanobe in Finland are some of the groups. Their main motive is to understand naonofluidics and nanosensing, to connect micro/nano eng. with biomedical and life science fields, to develop new micro and nano technologies for LoC, and to demonstrate new LoC applications. Developments of a Microfluidic LoCs have great potential to revolutionize the biomedical field and possess the capability to give a boost to healthcare sector. But still this LoC technology would seem to be a dream especially in developing countries. In the low-resource areas such as developing countries, efforts are still required to improve the business model under which LoC devices are produced and to make people aware about their efficient use. Many infectious diseases are there

such as malaria, HIV and AIDS, measles, TB, lower respiratory conditions and so on that require timely diagnosis and treatment so as to reduce the mortality rate. Now days, Swine Flu, Zika Virus and Ebola Virus are killing thousands of people and causing the risk of epidemic. For all these diseases, LoCs diagnostics are desperately needed because of their ability to provide diagnosis in real time so as to improve the disease-management landscape. Moreover, this technology can proven to be useful for finding a novel way to treat biomedical systems.

Objectives :

• Design of LoC and fabrication
• Design for microfluidic platform for single/multiple standardization biosensor chip • Characterization of microfluidic biosensor chip
• Development of microfluidics-integrated electrochemical immunosensing chip

Keywords :

graphene, lab-on-chip, microchannels, chamber structures.

Expected Output and Outcome of the proposal :

The developed low cost lab-on-chip can be highly useful for the medical diagnostics outside of traditional laboratory settings will likely be an important component of future health care. This will change the current trends in the biomedical manufacturing industries. Additionally, the proposed integrate knowledge of materials, instrumentation, control, rapid prototyping, and applied lab-on-chip in products with considerable near- term commercial potential and/or as appropriate technology for resource-limited areas of the world.