Dr.Pratikhya Raut

Designation : Assistant Professor
E-Mail ID : sweetpratikshya91@gmail.com
Contact at : EC-302, Department of Electronics and Communication Engineering,
Velagapudi Ramakrishna Siddhartha Engineering College,
Kanuru, Vijayawada, Andhra Pradesh 520007.
Mobile: 8249387167

Education

Ph. D (Microelectronics and VLSI Design)
2023., VIT-APUniversity,Andhra Pradesh

M.Tech (VLSI and Embedded System Design)
2017, BPUT, Odisha

B.Tech (Electronics and Communication Engineering)
2014, BPUT, Odisha

Experience

- Worked as a GIS mapping analyst in **Cognizant Technology Solution.**
  Place: **Hyderabad**
  Period**: March 2019- September 2020**

Research Interests

Broad Area of Research :

- Semiconductor Device Modeling
- Junctionless Field Effect Transistors
- Tunnel FET Transistors
- FinFET
- Biosensors Design
- Low Power Devices

- TCAD Simulation

Honors and Awards

- Received Best Research Award at University Level 2022-23 at VIT-AP University.
- Received Best Research Poster Presentation **V-SAMSODH 2022** at VIT-AP University.

Courses Taught

- Basic Electronics
- Digital Logic Design
- Semiconductor Device Physics
- CMOS VLSI Design

Research Profile

Publications

The recent publications and research contributions can be viewed from the following URLs

Google Scholar	**https://scholar.google.com/citations?hl=en&user=2PxNU9AAAAAJ**
Scopus	**https://www.scopus.com/authid/detail.uri?authorId=57226812484**
ORCID	**https://orcid.org/0009-0004-8332-0604**
Research Gate	https://www.researchgate.net/profile/Pratikhya-Raut
LinkedIn	https://www.linkedin.com/in/dr-pratikhya-raut-50ab61141/?originalSubdomain=in

Projects Handled:

- "Simulation and Modeling of Gate All Around Junctionless FET (GAA-JLFET) for RFIC Applications **(Ph.D. work)**
- "Determination of Interface Defect Densities in SiO_2 and High-k MOS Capacitor" (**MTech Project work**)
- **"**Image Processing Using Unified Learning Kit.**" (BTech Project work)**
- "MDIO UC Development
- Dual Port RAM Verification in system Verilog and UVM.

Research Publications in International Journals:

[1] ***Raut, P.,*** *Nanda,* ***U.*** *and Panda, D. K. (2023). "Analytical Drain Current Model Development of Twin Gate TFET in Subthreshold and Super Threshold Regions",* ***Microelectronics Journal- SCI-1.992*** **https://doi.org/10.1016/j.mejo.2023.105761**

[2] ***Raut, P.****, Nanda, U. and Panda, D. K. (2023) "Recent Trends on Junction Less Field Effect Transistors (JLFET) in terms of Device Topology, Modeling and Application",* ***ECS Journal of Solid State Science and Technology (SCI, IF: 2.070) doi:10.1149/2162-8777/acc35a (SCI-2.07)***

[3] ***Raut, P****., Nanda, U., &* Panda, D. K. *(2022). "RF with linearity and non-linearity parameter analysis of gate all around negative capacitance junction less FET (GAA-NC-JLFET) for different ferroelectric thickness",* ***Physica Scripta, 97(10), 105809. (SCI-3.08) doi: 10.1088/1402-4896/ac90fa***

[4] ***Raut, P****., & Nanda, U. (2022). "A Charge-Based Analytical Model for Gate All Around Junction-Less Field Effect Transistor Including Interface Traps",* ***ECS Journal of Solid State Science and Technology, 11(5), 051006. (SCI-2.07) doi:10.1149/2162-8777/ac6d7a***

[5] ***Raut, P****., & Nanda, U. (2022). "RF and linearity parameter analysis of junction-less gate all around (JLGAA) MOSFETs and their dependence on gate work function",* ***Silicon, 14(10), 5427-5435. (SCI-2.941) https://doi.org/10.1007/s12633-021-01312-z***

Book Chapter Published:

1. ***Raut, P****., Nanda, U. and Panda, D. K " Analysis of RF with DC and Linearity Parameter and study of Noise characteristics of Gate- All- Around Junctionless FET (GAA-JLFET) and its applications" accepted as book chapter in book"* ***Nano-Devices for IC Design.***
   https://doi.org/10.1002/9781394186396.ch6

Research Publications in International Conferences

1. **Raut, P.,** Nanda, U., & Panda, D. K. (2023, April). Design and Modeling of a Label-free JLTFET Based Biosensor for Enhanced Sensitivity in **2023 IEEE Devices for Integrated Circuit (DevIC) (pp. 77-81). IEEE.**
2. **P. Raut,** U. Nanda, D. K. Panda and H. P. T. Nguyen, "Design and Comparison of Wideband Cascode Low Noise Amplifier using GAA-JLFET and GAA-NC-JLFET for RFIC Applications" ***2023 2nd International Conference on Artificial Intelligence and Signal Processing (AISP)*****, 2023.**
3. **P. Raut,** U. Nanda, D. K. Panda and Chih-Chieh Hsu, "Performance Analysis of Double Gate Junctionless TFET with respect to different high-k materials and oxide thickness," ***2022 2nd International Conference on Artificial Intelligence and Signal Processing (AISP)*****, 2022,** pp. 1-5, doi: 10.1109/AISP53593.2022.9760584. *(Scoupus)*

4. Kumar, S. S., Prasad, A., Sinha, A., **Raut, P**., Das, P., Mahato, S. S., & Mallik, S. (2016, May). Impact of post metal annealing on gate work function engineering for advanced MOS applications. ***In AIP Conference Proceedings (Vol. 1728, No. 1, p. 020218). AIP Publishing LLC. (Scopus)***

FDP's/ Workshops/ Webinars/ Guest Lectures attended:

- Participated in 5 days offline FDP on "Universal Human Values: from 16/06/2023 - 20/06/2023, organized by the Department of ECE at Vignan University, Vadlamudi, Andhra Pradesh.
- Participated in 6 days AICTE Training And Learning (ATAL) Academy offline FDP on "Novel Materials, Devices and Applications" from 11-12-2023 to 16-12-2023 at VR Siddhartha Engineering College (Autonomous), Vijayawada.
- Participated in 3 days SERB sponsored National Workshop on "The Next Generation VLSI & MEMS Devices in medicine" from 20-12-2023-22-12-2023 at VR Siddhartha Engineering College (Autonomous), Vijayawada.

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