SKILL ORIENTED COURSE 2

DIGITAL SYSTEM DESIGN USING FPGA

Vivado Tutorial

Lab1 - Modelling Concepts

Lab2 - Numbering Systems

Lab3 - Multi-Output Circuits

Lab4 - Tasks, Functions, and Test bench

Lab5 - Modelling Latches and Flip-Flops

Lab6 - Modelling Registers and Counters

Lab7 - Behavioural Modelling and Timing Constraints

Lab8 - Architectural Wizard and IP Catalog

Lab9 - Counters, Timers, and Real-Time Clock

Lab10 - Finite State Machines

Lab11 - Sequential System Design using ASM Charts

Lab12- Create your own IPI block

SOFTWARE: XILINX VIVADO

HARDWARE: NEXYS 7 DEVELOPMENT BOARD

ROOM NO: 425, MICROCONTROLLERS & EMBEDDED SYSTEMS LAB
EIE DEPARTMENT

DATE	TIME
MONDAY	9:00 AM TO 12:00 PM
WEDNESDAY	2:00 PM TO 5:00 PM
THURSDAY	2:00 PM TO 5:00 PM
SATURDAY	9:00 AM TO 12:00 PM