VELAGAPUDI RAMAKRISHNA

SIDDHARTHA ENGINEERING COLLEGE

ELECTRONICS AND COMMUNICATION ENGINEERING

Curriculum, Scheme of Examination and Syllabi

for

M.TECH DEGREE PROGRAM

in

VLSI DESIGN AND EMBEDDED SYSTEMS

[M.TECH 19]

FIRST SEMESTER

w.e.f 2019-2020

Contact Hours: 23

S. No	Course Category	Course Code	Title of the Course	L	P	C	I	E	T
1.	Programme Core - I	19ECVE1001	Digital System Design using Programmable Devices	3	0	3	40	60	100
2.	Programme Core - II	19ECVE1002	ARM Controllers for Embedded Systems	3	0	3	40	60	100
3.	Programme Core - III	19ECVE1003	Device Modelling	3	0	3	40	60	100
4.	Programme Elective - I	19ECVE1014/1	VLSI Technology	3	0	3	40	60	100
		19ECVE1014/2	Sensors and Actuators						
		19ECVE1014/3	MEMS						
		19ECVE1014/4	Open/Industry offered elective						
5.	Programme Elective - II	19ECVE1015/1	Programming Languages for Embedded Software	3	0	3	40	60	100
		19ECVE1015/2	Advanced Computer Architecture						
		19ECVE1015/3	Advanced Signal Processing						
		19ECVE1015/4	Open /Industry offered elective						
6.	Mandatory Learning Course	19ECVE1026	Research Methodology and IPR	2	0	0	40	60	100
7.	Laboratory - I	19ECVE1051	Digital System Design Lab	0	3	1.5	40	60	100
8.	Laboratory - II	19ECVE1052	Embedded Systems Design Lab	0	3	1.5	40	60	100
			Total	**17**	**6**	**18**	**320**	**480**	**800**

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[M.TECH 19]
SECOND SEMESTER

Contact Hours: 25

S. No	Course Category	Course Code	Title of the Course	L	P	C	I	E	T
1.	Programme Core – IV	19ECVE2001	Real Time Operating Systems	3	0	3	40	60	100
2.	Programme Core – V	19ECVE2002	VLSI Design Verification	3	0	3	40	60	100
3.	Programme Core – VI	19ECVE2003	Analog & Mixed Signal Design	3	0	3	40	60	100
4.	Programme Elective – III	19ECVE2014/1	Low Power VLSI	3	0	3	40	60	100
		19ECVE2014/2	VLSI Signal Processing						
		19ECVE2014/3	Algorithms for VLSI						
		19ECVE2014/4	Open/ Industry offered elective						
5.	Programme Elective – IV	19ECVE2015/1	System Design with Embedded Linux	3	0	3	40	60	100
		19ECVE2015/2	Communication Busses and Interfaces						
		19ECVE2015/3	Parallel Processing						
		19ECVE2015/4	Open/ Industry offered elective						
6.	Audit Course	19ECVE2036	Technical Report Writing	2	0	-	-	-	-
7.	Term Paper	19ECVE2067	Term Paper seminar – Literature Review for the proposed problem#	2	0	1	40	60	100
8.	Laboratory - I	19ECVE2051	Real Time Operating Systems Lab	0	3	1.5	40	60	100
9.	Laboratory - II	19ECVE2052	Analog & Mixed Signal Design Lab	0	3	1.5	40	60	100
			Total	**19**	**6**	**19**	**320**	**480**	**800**

*****Students to be encouraged to go industrial training for at least Six weeks during semester break

#Students should conduct the Literature Survey for the proposed research topic and they need to develop a prototype or simulation based (must be outcome oriented) – the same to be presented in any conference (national or international)

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THIRD SEMESTER

Contact Hours:21

S. No	Course Category	Course Code	Title of the Course	L	P	C	I	E	T
1.	Programme Elective - V	19ECVE3011	Choice for students to complete course in any MOOCS Platform	3	0	3	-	-	100
2.	Project (Part-A)	19ECVE3062	Dissertation*/ Project/ Research Organization	0	18	10	40	60	100
3.	Internship	19ECVE3051	Internship/Summer Training in Research Organizations/ Institutions of Higher Learning (After II Sem)	0	0	2	-	-	100
			Total	**3**	**18**	**15**	**40**	**60**	**300**

*To be continued in the IV Semester

Program Elective V may be completed in semester I or II by satisfying the pre-requisites those who are going for industrial project

FOURTH SEMESTER

Contact Hours:32

S. No	Course Category	Course Code	Title of the Course	L	P	C	I	E	T
1.	Project (Part-B)	19ECVE4061	Dissertation/ Industrial Project	0	32	16	40	60	100
			Total	**0**	**32**	**16**	**40**	**60**	**100**

Total Credits:68

L – Lecture, P – Practical, C – Credits, I: Internal Assessment Marks, E: End Examination Marks, T: Total Marks

19ECVE1001: DIGITAL SYSTEM DESIGN USING PROGRAMMABLE DEVICES

Course Category:	Programme Core	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Digital Circuits	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Comprehend various PLDs and issues related to implementing digital systems in FPGA				
	CO2	Design applications using state machine for sequencing the operations in a digital system.				
	CO3	Understand basic techniques for testing combinational and sequential logic and representation of floating point numbers.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H				
	CO2				H	
	CO3					H

Course Content

UNIT I: (10 Hrs)

Review of Logic Design – Hazards in Combinational Circuits, Mealy Sequential Circuit Design, Design of a Moore Sequential Circuits, Sequential Circuit Timing, Tristate Logic and Busses.

Introduction to Programmable Logic Devices - Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II: (10 Hrs)

Field Programmable Gate Arrays - Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs, Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs, Dedicated Memory in FPGAs, Dedicated Multipliers in FPGAs, Cost of Programmability, FPGAs and One-Hot State Assignment, FPGA Capacity: Maximum Gates versus Usable Gates, Design Translation (Synthesis).

	UNIT III: **(15 Hrs)** **Design Examples** -A BCD Adder, 32-Bit Adders, Traffic Light Controllers, State Graphs for Control Circuits, Scoreboard and Controller, Synchronixation and Debouncing, A Shift-and-Add Multiplier, Array Multiplier, A Signed Integer/Fraction Multiplier, Keypad Scanner, Binary Dividers. **UNIT – IV:** **(15 Hrs)** **Floating-Point Arithmetic-** Representation of Floating-Point Numbers, Floating-PointMultiplication, Floating-PointAddition **Hardware Testing and Design for Testability -** Testing Combinational Logic, Testing Sequential Logic, Scan Testing, Boundary Scan, Built-InSelf-Test.
Text books and Reference books	**Text Books:** 1. Charles Roth, Lizy K. John, ByeongKil Lee - Digital Systems Design Using Verilog-CL Engineering (2015). **Reference Books:** 1. Michael D. Ciletti (2011), "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI, 2nd edition. 2. Palnitkar, S. (2010). Verilog HDL: A guide to digital design and synthesis (Vol. 1). Prentice Hall Professional,2nd edition. 3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
E-resources and other digital material	1. https://www.sciencedirect.com/topics/engineering/field-programmable-gate-arrays 2. https://faculty.kfupm.edu.sa/COE/mayez/ps-coe202/core/Lesson6_1.pdf 3. https://nptel.ac.in/courses/117108040/ 4. https://www.eng.auburn.edu/~nelsovp/courses/elec4200/Slides/Programmable%20Logic%20Devices.pdf

Name of Course Coordinator : Mr G Kishore Kumar

19ECVE1002: ARM CONTROLLERS FOR EMBEDDED SYSTEMS

Course Category:	Programme Core	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Computer Organization	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Understand and analyze the design aspects, Architecture, and instruction set associated with ARM processors.				
	CO2	Analyze the C programming optimization methods for ARM processor.				
	CO3	Examines various cache-technologies that surround the ARM cores.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1			M		
	CO2				M	
	CO3					L

Course Content

UNIT I: (12 Hrs)

ARM Processor Fundamentals: ARM Design Philosophy, Registers, CPSR, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions.

Introduction to the ARM Instruction Set: Data Processing Instructions, Branch Instructions, Load –Store Instructions, Software Interrupt Instruction, PSR Instructions.

Introduction to the Thumb Instruction Set: Thumb Register Usage, Branch Instructions, Data Processing Instructions, Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT II: (12 Hrs)

Efficient C Programming: Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Structure Arrangement.

Writing and Optimizing ARM Assembly Code: Writing Assembly Code, Profiling and Cycle Counting, Instruction Scheduling, Register Allocation, Conditional Execution, Looping Constructs.

UNIT III: (10 Hrs)

Exception and Interrupt Handling: Exception Handling, Interrupts, Interrupt Handling Schemes

Caches : The Memory Hierarchy and Cache Memory, Cache Architecture,

	Cache Policy, Fuhsing and Cleaning Cache Memory. **UNIT – IV:** (10 Hrs) **Memory Protection Units :** Protected Regions, Initializing the MPU, Caches and Write Buffer. **Memory Management Units:** Moving from an MPU to an MMU, How Virtual Memory Works, Details of the ARM MMU, Page Tables, Translation Lookaside Buffer, Domains And Memory Access Permission, The Fast Context Switch Extension
Text books and Reference books	**Text Books:** 1. A.Sloss, D.Symes, C.Wright, "ARM system Developers Guide: Designing and Optimizing System Software", Morgan Kaufmann publishers, 2012. **Reference Books:** 1. Steve Furber, "ARM System on Chip Architecture", 2nd ed., Addison Wesley Professional,2000. 2. Valvano, J,"Embedded microcomputer systems: real time interfacing", 3rd Edition, Cengage Learning, 2011. 3. Frank Vahid, TonyGivargis, "Embedded System Design", J Wiley India,2005.
E-resources and other digital material	1. https://nptel.ac.in/courses/106105193/ 2. https://www.arm.com/resources/education/education-kits/efficient-embedded-systems

Name of Course Coordinator : Dr Shaik Fayaz Ahamed

19ECVE1003: DEVICE MODELLING

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Basics of semiconductor, Network concept, Basic of electronics devices	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course:					
	CO1	The student will be able to understand the physics of MOSFET operation and its characteristics.				
	CO2	The student will be able to analyze the SOI MOSFET and electrical characteristics.				
	CO3	The student will be gain ability to design and model the nanoscale transistor.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	L	L	H		
	CO2	L	L	H		
	CO3	H		H		
Course Content	**UNIT I:** (10 Hrs) **MOS Capacitor**:Energy band diagram of Metal-Oxide-Semiconductor capacitor(MOS), Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, low frequency and high frequency capacitor-voltage characteristics, Non-idealities in MOS, oxide fixed charges, interfacial charges, Midgap gate Electrode. **UNIT II:** (13 Hrs) **Physics of MOSFET:** Drift-Diffusion Approach for current-voltage analysis, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao&Sah Model, MOSFET two dimensional effects, High field and doping dependent mobility models, High field effects and MOSFET reliability issues (SILC,TDDB, & NBTI). **UNIT III:** (12 Hrs) **Silicon on Insulator MOSFET:** FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET, FDSOI-sub-threshold slope, Floating body effect, single transistor latch, ZRAM device, Bulk and SOI FET: discussions referring to the ITRS					

	UNIT – IV: (10 Hrs) **Nanoscale Transistors:** Diffusive, Quasi Ballistic & Ballistic Transports, Ballistic planer and nanowire-FET modeling: semi-classical and quantum treatments Advanced MOSFETs: Strain Engineered Channel materials, Mobility in strained materials, Electrostatics of double gate, and Fin-FET devices
Text books and Reference books	**Text Books:** 1. Sze, S. M., & Ng, K. K. (2006). Physics of semiconductor devices. John wiley& sons. **Reference Books:** 1. B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Pearson, (2016) 2. Arora, N. (2007). MOSFET modeling for VLSI simulation: theory and practice. World Scientific. 3. YannisTsividis (2010), Operation and Modeling of the MOS Transistor, Oxford University Press, 3rd edition
E-resources and other digital material	1. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-012-microelectronic-devices-and-circuits-fall-2009/lecture-notes/

Name of Course Coordinator : Dr. Aniruddh Bahadur Yadav

19ECVE1014/1: VLSI TECHNOLOGY

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Semiconductor Devices, Linear Integrated Circuits	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Appreciate the various techniques involved in the VLSI fabrication process.				
	CO2	Understand the different lithography methods, Oxidation and etching process.				
	CO3	Appreciate the deposition and diffusion mechanisms.				
	CO4	Understand the ion implantation and metallization process.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1			M		
	CO2			M		
	CO3				L	
	CO4			M		

Course Content

UNIT I: (10 Hrs)

Crystal Growth and Wafer Preparation – Introduction, Electronic grade silicon, Czochralski crystal growing, Silicon shaping, Processing considerations.

Epitaxy – Introduction, Vapor phase epitaxy, Molecular beam epitaxy, Silicon-on-insulators, Epitaxial evaluation.

UNIT II: (13 Hrs)

Oxidation – Introduction, Growth mechanism and kinetics, Thin oxides, Oxidation techniques and systems, Oxide properties, Redistribution of dopants at interface, Oxidation of polysilicon, Oxidation induced defects.

Lithography – Introduction, Optical lithography, Electron lithography, X-Ray lithography, Ion lithography.

Reactive Plasma Etching – Introduction, Plasma properties, Feature size control and anisotropic etch mechanisms, Reactive plasma etching techniques and equipment.

UNIT III: (12 Hrs)

Dielectric and Polysilicon Film Deposition – Introduction, Deposition processes, Polysilicon, Silicon dioxide, Silicon nitride, Plasma assisted depositions.

	Diffusion – Introduction, Models of diffusion in solids, Measurement techniques, Diffusion in polycrystalline silicon, Diffusion in SiO2. **UNIT – IV:** (10 Hrs) **Ion Implantation** – Introduction, Range theory, Implantation equipment, Annealing, Shallow junctions, High-energy implantation. **Metallization** – Introduction, Metallization applications, Metallization choices, Physical vapor deposition, Patterning.
Text books and Reference books	**Text Books:** 1. S.M.Sze, "VLSI Technology (2nd edition)" , McGraw Hill, 2003 2. W. Wolf, "Modern VLSI Design", (3rd edition), Pearson,2002 **Reference Books:** 1. Plummer (2001), "Silicon VLSI Technology: Fundamentals, Practice, and Modeling", Pearson Education India. 2. C.Y. Chang and S.M.Sze (Ed), (1996), "ULSI Technology", McGraw Hill Companies Inc. 3. Stephen Campbell (2012), "The Science and Engineering of Microelectronics", Oxford University Press,.
E-resources and other digital material	1. Lecture Series on VLSI Design by Dr.NanditaDasgupta, Department of Electrical Engineering, IIT Madras. For more details on NPTEL visit http://nptel.ac.in 2. https://www.youtube.com/watch?v=Hp4xFkEZUos&list=PL5060CE8F13023479Video lecture series from IIT Professors VLSI Technology by Prof.SantiramKal, IIT KGP

Name of Course Coordinator : Dr. M. Durga Prakash

19ECVE1014/2 SENSORS AND ACTUATORS

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Basics of sensor and actuator, thin film and design	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course the student will be able to:					
	CO1	understand the fundamentals of material, and micro/nano device synthesis				
	CO2	apply knowledge of mathematics, science, and engineering to identify and solve the engineering problem				
	CO3	familiarized with micro electrical mechanical devices for optical, pressure sensor, force sensor and other interdisciplinary application				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	L	L	H		
	CO2	H				
	CO3	L	L	H		

Course Content

UNIT I: (9 Hrs)

Materials for Sensors and Actuators Materials. Substrates. Additive Materials.

Fabrication Techniques of Sensors and Actuators

Deposition. Lithography. Etching. Thin film fabrication: chemical vapor deposition, thermal evaporation, focused ion beam etching and deposition, LIGA. Wafer bonding

UNIT II: (8 Hrs)

Sensors characteristics

Transfer function: Mathematical Models, Sensitivity, Multidimensional Transfer Functions, Calibration. Span (Full-Scale Input). Full-Scale Output. Accuracy. Calibration Error. Nonlinearity

UNIT III: (12 Hrs)

MEMS Technology Pressure Sensors

Micromachined Silicon Diaphragms. Piezoresistive Pressure Sensors. Capacitive Pressure Sensors. Microphones.

MEMS Technology for Force sensor

Resonant and SAW Devices. Optical Devices. Capacitive Devices. Magnetic Devices. Atomic Force Microscope and Scanning Probe. Tactile Sensor.

	MEMS Technology for Flow sensor Pressure Difference Flow Sensors. Flow Sensor Based on the Faraday Principl. Turbulent Flow Studies. Nonthermal Time of Flight Flow Sensors Electrohydrodynamic. Electrochemical **UNIT – IV:** (11 Hrs) **Transduction Technique** Piezoresistivity. Piezoelectricity. Capacitive Techniques. Optical Techniques. Intensity Phase Wavelength. Spatial Position. Frequency. Polarization. Resonant Techniques. Vibration Excitation and Detection Mechanisms. Resonator Design Characteristics. **Actuation Technique** Actuation Techniques. Electrostatic. Piezoelectric. Thermal, Magnetic.
Text books and Reference books	**Text Books:** 1. Stephen Beeby Graham Ensell Michael Kraft Neil White, MEMS Mechanical Sensors, Artech House, Inc. Boston London www.artechhouse.com 2. Jacob Fraden, Handbook of Modern Sensors, fith edition Springer **Reference Books:** 1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics", Cambridge University Press, 2008. (ISBN: 9781107403765)
E-resources and other digital material	1. https://application.wileyvch.de/vch/journals/2081/books/2081_rel_title_varadan.pdf

Name of Course Coordinator : Dr. Aniruddh Bahadur Yadav

19ECVE1014/3 MEMS

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Semiconductor Devices, Analog Electronics Circuits Design	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	To understand the basic concepts of MEMS technology and working of MEMS devices.				
	CO2	To understand and selecting different materials for current MEMS devices and competing technologies for future applications.				
	CO3	To understanding the concepts of fabrication process of MEMS, Design and Packaging Methodology.				
	CO4	To analyze the various fabrication techniques in the manufacturing of MEMS Devices.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1			M		
	CO2				M	
	CO3			M		
	CO4				M	

Course Content

UNIT I: (10 Hrs)

Introduction to MEMS: Overview of MEMS and Microsystem- Typical MEMS and Microsystem Products, Evolution of Microfabrication, Microsystem and Microfabrication, Applications of Microsystems. Working principles of Microsystems- Microsensors, Microactuation, MEMS with Microactuation, Microaccelertometers, Microfludics.

UNIT II: (13 Hrs)

MEMS Materials and Their Properties: Scaling Laws in Miniaturization- Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic forces, Scaling in Electromagnetic forces, Scaling in Electricity, Scaling in Fluidic Mechanics. Materials for MEMS and Microsystems- Substrates and Wafers, Actives Substrates materials, Silicon Compounds, Silicon Piezoresistors, Gallium Arsenide, Quartz, Piezoelectric crystals, Polymers, Packaging materials.

UNIT III: (12 Hrs)

MEMS Fabrication Processes: Microsystem Fabrication Process- Photolithography, Ion Implantation, Diffusion, Oxidation, CVD, PVD,

	Deposition by Epitaxy, Etching. Overview of Micromanufacturing- Bulk Micromanufacturing, Surface Micromanufacturing, LIGA Process. **UNIT – IV:** (10 Hrs) **MEMS Devices**: Microsystems Design- Design Considerations, Process Design, Mechanical Design, Mechanical Design using FEM, Design of a Silicon Die for a Microprocessor Sensor, Design of Microfulidic Network Systems, Design Case Studies on Applications- Cantilevers, Microheaters,Accelerometers, Pressure Sensors, Micromirrors in DMD, Inkjet printer-head.
Text books and Reference books	**Text Books:** 1. Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture", Tata McGraw Hill, (2002). **Reference Books:** 1. An Introduction to Microelectromechanical Systems Engineering; 2nd Ed - by N.Maluf, K Williams; Publisher: Artech House Inc. 2. Fundamentals of Microfabrication - by M. Madou; Publisher: CRC Press; 2 edition 3. Stephen D. Senturia, "Microsystem Design", Springer International Edition, (2010).
E-resources and other digital material	1. Lecture Series on MEMS & Microsystems by Prof. Santiram Kal, Department of Electronics & Electrical Communication Engineering, I.I.T,Kharagpur. For More details on NPTEL visit http://nptel.iitm.ac.in 2. https://www.youtube.com/watch?v=EALXTht-stg

Name of Course Coordinator : Dr. M. Durga Prakash

19ECVE1015/1: PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Microprocessors and Microcontrollers	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Write an embedded C application of moderate complexity.				
	CO2	Ability to develop programs using object-oriented concepts.				
	CO3	Develop and analyze algorithms in C++.				
	CO4	Differentiate interpreted languages from compiled languages.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H				
	CO2		M		M	
	CO3			M		
	CO4					L

Course Content

UNIT I: (12 Hrs)

Embedded ‘C’ Programming - Bitwise operations, Dynamic memory allocation, OS services - Linked stack and queue, Sparse matrices, Binary tree - Interrupt handling in C, Code optimization issues - Writing LCD drives, LED drivers, Drivers for serial port communication - Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT II: (12 Hrs)

Object Oriented Programming - Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism, CPP Programming: ‘cin’, ‘cout’, formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, ‘this’ pointer, constructors, destructors, friend function, dynamic memory allocation.

UNIT III: (15 Hrs)

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual

	functions, Templates: Function template and class template, member function templates and template arguments,Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. **UNIT – IV:** (10 Hrs) Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.
Text books and Reference books	**Text Books:** 1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008. 2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011. 3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002 4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999. 5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005. **Reference Books:** 1. Programming embedded systems II by Michel J Pont.
E-resources and other digital material	1. "C programming for embedded microcontroller systems", V.P. Nelson.

Name of Course Coordinator : R V H Prasad, Assistant Professor

19ECVE1015/2: ADVANCED COMPUTER ARCHITECTURE

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Digital Electronics, Computer Architecture, Microprocessor and Micro controllers	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Describe the computer architecture pipelining and pipeline hazards				
	CO2	Provide process of organization and management of cache memory to yield high-performance from processors				
	CO3	Understood the memory storage process and technology				
	CO4	Analyze the parallel processing and multi core technology of a computer system				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M		M		
	CO2	M			M	M
	CO3	H	L	H		M
	CO4	H	M	H	M	M

Course Content

UNIT I: (9 Hrs)

Logic design conventions, building a datapath, an overview of pipelining, pipelined datapath and control, data hazards, forwarding vs stalling, control hazards, exceptions.

UNIT II: (9 Hrs)

Basics of cache organization, measuring and improving cache performance, virtual memory, using a finite state machine to control a simple cache, parallelism and memory hierachy: cache coherence.

UNIT III: (9 Hrs)

Dependability, reliability and availability, disk storage, flash storage, connecting processors, memory and IO devices, interfacing IO devices to the processor, memory and operating system, I/O performance measures: example for disk and fille systems. Design and IO system, parallelism and IO: redundant arrays of in expensive disks.

	UNIT – IV: (9 Hrs) The difficulty of creating parallel processing programs, shared memory multiprocessors, clusters and other message-passing multiprocessors, hardware multithreading, SISD, MIMD, SIMD,SPMD and vectors, introduction to graphics processing units, introduction to network processor network topologies, multiprocessor benchmarks, roofline simple performance model.
Text books and Reference books	**Text Books:** 1. Patterson, D. A., & Hennessy, J. L. (2013). Computer organization and design MIPS edition: the hardware/software interface. Newnes. **Reference Books:** 1. Kai Hwang and A.Briggs (1984) "Computer Architecture and parallel Processing" International Edition McGraw-Hill. 2. DezsoSima, Terence Fountain, Peter Kacsuk (1997), "Advanced Computer Architectures", Pearson.
E-resources and other digital material	1. https://swayam.gov.in/nd1_noc19_cs62/preview 2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-823-computer-system-architecture-fall-2005/

Name of Course Coordinator: R V H Prasad, Assistant Professor

19ECVE1015/3: ADVANCED SIGNAL PROCESSING

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Digital signal processing	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Design a sample rate converter that reduces/increase by a given factor.				
	CO2	Analyze and synthesize FIR filter for given multistructure filter bank				
	CO3	Evaluate the Optimum reflection coefficients for the Lattice Forward and Backward Predictors				
	CO4	Understand the concepts of LMS and RLS algorithms				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1				M	
	CO2				M	
	CO3			M		
	CO4			M		

Course Content

UNIT – I

Multirate Digital Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling Rate Conversion by a Rational Factor I/D, Implementation of Sampling Rate Conversion: Polyphase Filter Structures, Interchange of Filters and Downsamplers/Upsamplers, Sampling Rate Conversion with Cascaded Integrator Comb Filters, Polyphase Structures for Decimation and Interpolation Filters, Structures for Rational Sampling Rate Conversion

UNIT – II

Multistage FIR Filter Design: Multistage Implementation of Sampling Rate Conversion, Applications of Multirate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrowband Low pass Filters, Sub band Coding of Speech Signals, Digital Filter Banks: Poly phase Structures of Uniform Filter Banks, Transmultiplexers, Two channel Quadrature Mirror Filter Bank: Elimination of aliasing, Condition for Perfect reconstruction, Polyphase form of the QMF Bank

UNIT – III

Linear Prediction : Forward and Backward Linear Prediction – Forward

	Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters **UNIT –IV** **Adaptive Filters:** Applications of Adaptive Filters: System Identification or System Modeling, Adaptive Channel Equalization, Echo Cancellation in Data Transmission over Telephone Channels, Suppression of Narrowband Interference in a Wideband Signal, Adaptive Noise Cancelling, Linear Predictive Coding of Speech Signals, Adaptive Arrays. Adaptive Direct Form FIR Filters – The LMs Algorithm: Minimum Mean Square Error Criterion, The LMS Algorithm, Related Stochastic Gradient Algorithms, Properties of the LMS Algorithm.
Text books and Reference books	**TEXTBOOKS:** 1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.(Units-I,II,III & IV) **REFERENCES:** 1. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education 2. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH
E-resources and other digital material	1. https://nptel.ac.in/courses/108105055/ 2. http://nptel.iitm.ac.in/courses/Webcourse-contents/IITKANPUR/Digi_Sign_Pro/ui/TOC.htm

Name of Course Coordinator : Dr. N.S.Murthy

19ECVE1051: DIGITAL SYSTEM DESIGN LAB

Course Category:	Laboratory	**Credits:**	1.5
Course Type:	Practical	**Lecture - Tutorial -Practice:**	0-0-3
Prerequisites:	Digital Design	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Get acquainted with programmable logic design flow.				
	CO2	Implement designed digital circuits using FPGA.				
	CO3	Synthesize the designed circuits using CAD tools				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H				
	CO2				H	
	CO3					H
Course Content	**List of Experiments** 1. Design a BCD to 7-segment Decoder 2. Design a BCD Adder 3. Deasign 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats. 4. Design a Mealy and Moore Sequence Detector to detect a Sequence. 5. Design a Traffic Light Controller 6. Design a Score board controller 7. Design a Signed Integer/ Fraction Multiplier 8. Design a Binary Divider. 9. Design a BCD to excess 3 code converter 10. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.					

Name of Course Coordinator :G Kishore Kumar

19ECVE1052: EMBEDDED SYSTEMS DESIGN LAB

Course Category:	Laboratory	**Credits:**	1.5
Course Type:	Practical	**Lecture - Tutorial -Practice:**	0-0-3
Prerequisites:		**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Design and execute the different concepts for embedded system using ARM processor				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1				M	
Course Content	**I. Experiments using ARM-:** 1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division b. Operating Modes, System Calls and Interrupts c. Loops, Branches 2. Program to configure and control General Purpose Input / Output (GPIO) port pins. 3. Programs to read digital values from external peripherals and execute them with the Target board. 4. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment 5. Program to demonstrate Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program. 6. Program to demonstrate a simple interrupt handler and setting up a timer. 7. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal. 8. Program to demonstrate ADC interfacing 9. Program to demonstrate I2C Interface on IDE environment 10. Generation of PWM Signal 11. Development of simple firmware for small scale acquisition system.					

Name of Course Coordinator : Dr Shaik Fayaz Ahamed

19ECVE2001: REAL TIME OPERATING SYSTEMS

Course Category:	Programme Core	**Credits:**	03
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Embedded Systems concepts and Operating System	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Illustrate real time programming concepts				
	CO2	Apply RTOS functions to implement embedded applications				
	CO3	Relate RTOS roles to real time applications				
	CO4	Understand fundamentals of design consideration for embedded applications				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1			M		M
	CO2	M		L		
	CO3	H		M	M	M
	CO4	H		M	M	M

Course Content

UNIT I: (9 Hrs)

Introduction to Real-Time Operating Systems - Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS

Task- Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency

UNIT II: (9 Hrs)

Semaphores - Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use

Message Queues - Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables

UNIT III: (9 Hrs)

Exceptions and Interrupts - Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts

	Timer and Timer Services - Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines. **I/O Subsystems -** I/O concepts, I/O subsystems **UNIT – IV:** (9 Hrs) **Synchronization and Communication -** Synchronization, Communication, Resource Synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns, **Common Design Problems -** Resource Classification, Deadlocks, Priority Inversion
Text books and Reference books	**Text Books:** 1. Qing Li, Caroline Yao (2003), "Real-Time Concepts for Embedded Systems", CMP Books **Reference Books:** 1. Albert Cheng, (2002), "Real-Time Systems: Scheduling, Analysi Verification", Wiley Interscience. 2. Hermann Kopetz, (1997), "Real-Time Systems: Design Principle Distributed Embedded Applications", Kluwer. 3. Insup Lee, Joseph Leung, and Sang Son, (2008) "Handbook of Real Systems", Chapman and Hall. 4. Krishna and Kang G Shin, (2001), "Real-Time Systems", McGraw Hill
E-resources and other digital material	1. https://nptel.ac.in/courses/106105036/ 2. https://nptel.ac.in/noc/individual_course.php?id=noc18-cs12

Name of Course Coordinator :R V H Prasad

19ECVE2003: VLSI DESIGN VERIFICATION

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Verilog HDL	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Familiarity of the front end design and verification techniques				
	CO2	Apply System Verilog constructs to create reusable test environments.				
	CO3	Understand OOP concept in System Verilog				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M				
	CO2				M	
	CO3	M			M	
Course Content	**UNIT I: (10 Hrs)** **Verification Guidelines:** Verification process, Basic Testbench functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Functional coverage, Testbench components, Layered Testbench, Building layered Testbench, Simulation Environment phases, Maximum code reuse, Testbench performance. **UNIT II: (12 Hrs)** **Data Types:** Built in data types, Fixed sized arrays, Dynamic arrays, Queues, Associative Arrays, Linked lists, Array methods, Choosing a storage data type, Creating new types with typedef, Creating user defined structures, Type conversion, Enumerated types, Constant strings, Expression width **UNIT III: (12 Hrs)** **Procedural statements and routines:** Procedural statements, tasks, Functions, Routine Arguments, Returning from a routine, Local data storage, Time values **Connecting the Testbench and Design:** Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling,					

	connecting it all together, Top level scope program – Module interactions. **UNIT – IV: (12 Hrs)** **System Verilog Assertions:** Immediate Assertions, Customizing the Assertion Actions, Concurrent Assertions, Exploring Assertions. **Basic OOP:** Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, creating new objects, Object De-allocation using objects, Static variable vs Global variable, Class methods, Defining methods outside of the class, Scoping rules, using one class inside another, Understanding dynamic objects, Public vs. Local, Straying offcourse building a testbench.
Text books and Reference books	**Text Books** 1. Chris Spears, "System Verilog for Verification", Springer, 2nd Edition. **Reference Books** 1. M. Bushnell and V.D. Agarwal "Essential of electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publisher.
E-resources and other digital material	1. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog – Unified Hardware Design, Specification and Verification Language). 2. System Verilog website – www.systemverilog.org

Name of Course Coordinator: G. Venkata Subbaiah**.**

19ECVE2003: ANALOG & MIXED SIGNAL DESIGN

Course Category:	Programme Core	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Analog Electronics Circuits Design.	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Design single stage amplifiers and Op-Amp amplifiers.				
	CO2	Analyze feedback amplifiers and oscillators.				
	CO3	Analyze the analog-digital converters and Comparators.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1			M		
	CO2				M	
	CO3			M		

Course Content

UNIT I: (10 Hrs)

Single Stage Amplifiers and Current Mirrors - Common source, common gate and source follower stages- Cascode and folded cascode structures- Frequency response, MOS current mirrors-sources.

UNIT II: (13 Hrs)

MOS Differential Amplifiers and Operational Amplifiers - Single ended and differential operation, Basic differential pair, Common mode response, Frequency response- CMOS operational amplifiers - One-stage op-amps and two stage op-amps.

UNIT III: (12 Hrs)

Feedback Amplifiers - General considerations, Feedback topologies, Oscillators and PLLs – General Considerations, Ring oscillators, LC oscillators, Voltage controlled oscillators, Basics of PLLs.

UNIT – IV: (10 Hrs)

Switched-Capacitor circuits – Sampling switches, Switched-Capacitor amplifiers, Switched-Capacitor integrator

Comparators and Analog-Digital converters – Two stage, Open-loop comparators, Parallel digital-analog converters.

Text books and Reference books	**Text Books:** 1. BehzadRazavi (2002), 'Design of Analog CMOS Integrated Circuits' Tata-McGrawHill. 2. Philip Allen & Douglas Holberg (2002), "CMOS Analog Circuit Design", Oxford University Press. **Reference Books:** 1. David A Johns & Ken Martin (2001), "Analog Integrated Circuit Design" John Wiley and Sons.
E-resources and other digital material	1. CMOS Analog VLSI Design by Prof. A.N. Chandorkar,Department of Electronics & Communication Engineering,IIT Bombay.For more details on NPTEL visit http://nptel.ac.in

Name of Course Coordinator : Dr. M. Durga Prakash

19ECVE2014/1: LOW POWER VLSI

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	VLSI Design	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Apply different circuit techniques to manage the leakage currents				
	CO2	Comprehend existing low power adder and multiplier architectures				
	CO3	Understand the architectural and circuit level techniques for attaining low power consumption				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M		H		
	CO2	M		H		
	CO3			M		
Course Content	**UNIT I:** (12 Hrs) **Low power CMOS VLSI design -** Introduction, sources of power dissipation, static power dissipation, active power dissipation. **Circuit techniques for low power design -** Introduction, designing for low power, circuit techniques for leakage power reduction **UNIT II:** (11Hrs) **Low voltage low power adders -** Introduction, standard adder cells, CMOS adder's architectures, low voltage low power design techniques, current mode adders. **Low voltage low power multipliers -** Introduction, overview of multiplication, types of multiplier architectures, braun multiplier, baugh-wooley multiplier, booth multiplier, wallace tree multiplier **UNIT III:** (12 Hrs) **Low voltage low power static RAM -** Basics of SRAM, memory cell, precharge and equalization circuit, decoder, address transition detection, sense					

	amplifier, output latch, low power SRAM technologies. **Low voltage low power dynamic RAM -** Types of DRAM, basics of DRAM, self refresh circuit, half voltage generator, voltage down converter, future trends and developments of DRAM **UNIT – IV:** (10 Hrs) **Low- Voltage Low Power Read-Only Memories -** Introduction, types of ROM, basics physics of floating gate nonvolatile devices, floating gate memories, basics of ROM, low power ROM Technology.
Text books and Reference books	**Text Books:** 1. KiatSeng Yeo, Kaushik Roy (2012),"Low Voltage, Low Power VLSI Subsystems", TATA McGraw-Hill. **Reference Books:** 1. Yeo Rofail,Gohl (2009)," CMOS/BiCMOS ULSI Low Voltage, Low Power", Pearson Education Asia 1st Indian reprint. 2. Anantha P. Chandrakasan, Robert W. Brodersen, " Low Power Digital CMOS Design", Springer Science 3. Jan M. Rabaey, Anantha P. Chandrakasan, BorivojeNikolic, (2011) "Digital Integrated Circuits: a Design Perspective", Pearson Education, 2nd Edition.
E-resources and other digital material	1. http://www.nptelvideos.com/course.php?id=422 2. http://leda.elfak.ni.ac.rs/education/projektovanjeVLSI/predavanja/10%20Low%20Power%20Design%20in%20VLSI.pdf 3. https://www.egr.msu.edu/classes/ece410/salem/files/s16/lectures/Ch2_S2_N.pdf

Name of Course Coordinator :K. Naga Sunanda

19ECVE2014/2: VLSI SIGNAL PROCESSING

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	VLSI Design, Digital Signal Processing	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Apply the concepts of pipelining, parallel processing, Retiming, Folding and unfolding to optimize digital signal processing architectures.				
	CO2	Analyze data flow in systolic architectures.				
	CO3	Minimize the computational complexity using fast convolution algorithms.				
	CO4	Analyze pipelining and parallel processing of IIR filters.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H	L	M		
	CO2	H	L	M		
	CO3	H	L	M	M	
	CO4	L	L	M		

Course Content

UNIT I (10Hrs)

Introduction to DSP - Typical DSP algorithms, Representations of DSP algorithms

Iteration Bound – Loop bound and Iteration bound, Algorithms for computing iteration bound.

Pipelining and Parallel Processing - Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power.

UNIT II (12Hrs)

Retiming - Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

Unfolding - Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming.

Folding - Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of Multirate systems

	UNIT III (15Hrs) **Systolic Architecture Design -** Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design. **Fast Convolution -** Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution **UNIT – IV** **(10Hrs)** **Pipelined and Parallel Recursive and Adaptive Filters –** Introduction - Pipeline Interleaving in Digital Filters, Pipelining in 1st-Order IIR Digital Filters, Pipelining in Higher-Order IIR Digital Filters, Parallel processing for IIR Filters, Combined Pipelining and Parallel Processing for IIR Filters.
Text books and Reference books	**Text Books:** 1. Keshab K. Parthi. (2013), "VLSI Digital Signal Processing- System Design and Implementation", Wiley Inter Science. **Reference Books:** 1. Jose E. France, Yannis Tsividis. (1994) "Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing", Prentice Hall. **2.** Medisetti V. K . (1995), "VLSI Digital Signal Processing", IEEE Press (NY), USA.
E-resources and other digital material	1. http://viplab.cs.nctu.edu.tw/ 2. http://people.ece.umn.edu/users/parhi/SLIDES/

Name of Course Coordinator: RajasekharTuraka

19ECVE2014/3: ALGORITHMS FOR VLSI

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Data structures (or discrete math) & logic design.	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Comprehend the working of physical design flow.				
	CO2	Formulate CAD design using algorithm paradigms				
	CO3	Formulate a problem with Floorplanning and Placement Algorithms				
	CO4	Understand design and automation of the FPGA's and MCM's.				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M				
	CO2				H	
	CO3				H	
	CO4					M
Course Content	**UNIT I: (15 Hrs)** **VLSI Physical Design Automation-**VLSI Design Cycle, Physical Design Cycle, New Trends, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools **Fabrication Process and Impact-**Fabrication Materials, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Design, Scaling Methods, Status of Fabrication Process, Issues related to Fabrication Process, Future of Fabrication Process, Tools and Process Development **UNIT II: (15 Hrs)** **Data Structures and Basic Algorithms-**Complexity Issues and N-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical Design **UNIT III: (15 Hrs)** **Partitioning-** Introduction to Partitioning, Problem Formulation, Classification of Partitioning Algorithm, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithm, Performance Drive Partitioning					

	UNIT – IV: (15 Hrs) **Routing and Automation of FPGA's and MCM's-**Global Routing, Detailed Routing, Clock Routing, Power and Ground Routing, Compaction, Physical Design Automation of the FPGA's and MCM''s.
Text books and Reference books	**Text Books:** 1. 1.Naveed A. Sherwani (1999), "Algorithms for VLSI Physical Design Automation, Third Edition, Kluwer Academic Publications. **Reference Books:** 1. S.H.Gerez (1998), "Algorithms for VLSI Design Automation", Wiley Publication. **2.** Sadiq M. Sait and Habib Youssef (1999), "VLSI Physical Design Automation: Theory and Practice" by World Scientific Publishers, Singapore/New-Jersey, USA. (Also published by McGraw-Hill Book Co., Europe, December 1995).
E-resources and other digital material	1. https://www.springer.com/gp/book/9780792383932 2. https://books.google.co.in/books?isbn=8126508213

Name of Course Coordinator: V B K L Aruna.

19ECVE2015/1 SYSTEM DESIGN WITH EMBEDDED LINUX

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Microcontrollers	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Illustrate linux programming concepts and embedded board support package.				
	CO2	Understand concepts of embedded storage and device drivers				
	CO3	Understand fundamentals of porting, building and debugging an embedded application				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M				
	CO2		M			
	CO3			M		

Course Content

UNIT I **(12 Hrs)**

Introduction-Why Embedded Linux?, Embedded Linux Versus Desktop, Embedded Linux Distributions, Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross-Platform Tool chain,

Board Support Package- Inserting BSP in Kernel Build Procedure, The Boot Loader Interface, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART , Power Management,

UNIT II **(12 Hrs)**

Embedded Storage- Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices, Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory

Embedded Drivers- Linux Serial Driver, Ethernet Driver, I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules,

UNIT III **(12 Hrs)**

Porting Applications- Architectural Comparison, Application Porting

	Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver **Building and Debugging**- Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems, Kernel Debuggers, Profiling, **UNIT – IV** **(12 Hrs)** **Embedded Graphics**- Graphics System, Linux Desktop Graphics—The X Graphics System, Introduction to Display Hardware, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications
Text books and Reference books	**Text Books** 1. Raghavan, P., Lad, A., & Neelakandan, S. (2005). Embedded Linux system design and development. CRC press. **Reference Books** 1. Barr, M., & Massa, A. (2006). Programming embedded systems: with C and GNU development tools., O'Reilly Media, Inc.
E-resources and other digital material	1. http://www.esys.ir/Files/Ref_Books/Linux/esys.ir_Embedded.Linux.System.Design.and.Development.pdf 2. https://opensource.com/article/18/6/embedded-linux-build-tools

Name of Course Coordinator: G. VenkataSubbaiah.

19ECVE2015/2: COMMUNICATION BUSSES AND INTERFACES

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Computer Networks	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Select a particular serial bus suitable for a particular application.				
	CO2	Develop APIs for configuration, reading and writing data onto serial bus.				
	CO3	Design and develop peripherals that can be interfaced to desired serial bus.				
	CO4	Explain the types of transmission media with real time applications				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H				
	CO2		M		M	
	CO3			M		
	CO4					L
Course Content	**UNIT I:** (12 Hrs) Serial Busses - Physical interface, Data and Control signals, features, **UNIT II:** (12 Hrs) Limitations and applications of RS232, RS485, I2 C, SPI, CAN - Architecture, Data transmission, Layers, Frame formats. **UNIT III:** (15 Hrs) CAN bus applications, USB - Transfer types, enumeration, Descriptor types and contents, Device driver. **UNIT – IV:** (10 Hrs) PCIe - Revisions, Configuration space, Hardware protocols, applications, Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable.					
Text books and Reference books	**Text Books:** 1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition					

	2. Jan Axelson, "USB Complete", Penram Publications 3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press 4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005. **Reference Books:** 1. Serial Front Panel Draft Standard VITA 17.1 – 200x
E-resources and other digital material	1. www.can-cia.org 2. www.pcisig.com 3. www.usb.org

Name of Course Coordinator : Dr Sk Fayaz Ahmed

19ECVE2015/3: PARALLEL PROCESSING

Course Category:	Programme Elective	**Credits:**	3
Course Type:	Theory	**Lecture - Tutorial -Practice:**	3-0-0
Prerequisites:	Computer Architecture and Organization	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Understand the evolution of High Performance Computing (HPC) with respect to laws and the contemporary notion that involves mobility for data, hardware devices and software agents				
	CO2	Understand, appreciate and apply parallel and distributed algorithms in problem Solving				
	CO3	Evaluate the impact of network topology on parallel/distributed algorithm formulations and traffic their performance.				
	CO4	Gain experience parallel and distributed programming techniques				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H				
	CO2				M	
	CO3				M	
	CO4					M
Course Content	**UNIT I:** (10 Hrs) Introduction to Parallel Computing Architectures, Parallel hardware, Parallel Software, Processes and threads, Programming models, Shared memory, Distributed memory, Amdahl's Law. **UNIT II:** (15 Hrs) Distributed memory programming with MPI:MPI Programs, SPMD Programs, Message matching, Trapezoidal rule in MPI, Parallelizing the trapezoidal rule, Parallel sorting algorithms. **UNIT III:** (12 Hrs) Shared memory Programming with Pthreads: Processes, Threads and Pthreads, Matrix Vector Multiplication, Read Write Locks, Caches, Cache coherence and false sharing, Thread Safety. **UNIT – IV:** (15 Hrs). Parallel Program Development:Parallelizing the solvers using Pthreads, Parallelizing the basic solver using MPI, Parallelizing the reduced solver using MPI, Performance of MPI solvers, Tree serarch					
Text books	**Text Books:**					

and Reference books	1. Peter S Pacheco, An Introduction to Parallel Programming, Morgan Kaufmann,2011. **Reference Books:** 1. M Herlihy and N Shavit, The Art of Multiprocessor Programming Morgan Kaufmann, 2008. 2. JL Hennessy and DA Patterson, Computer Architecture: A Quantitative Approach,4th Ed., Morgan Kaufmann/Els India, 2006.
E-resources and other digital material	1. https://www.sciencedirect.com › book › an-introduction-to-parallel-program.

Name of Course Coordinator :V B K L Aruna

19ECVE2051: REAL TIME OPERATING SYSTEMS LAB

Course Category:	Laboratory	**Credits:**	1.5
Course Type:	Practical	**Lecture - Tutorial -Practice:**	0-0-3
Prerequisites:	Micro controller and Embedded systems lab	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Design and execute the different RTOS concepts for embedded system design				
	CO2	Developing the RTOS application on Micro controller board				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	M	H	M	M	M
	CO2	M	H	M	M	M
Course Content	**I.Experiments using ARM with RTOS:** 1. Creating FreeRTOS Tasks 2. UART Printmsg implementation using stdperiph. libary 3. Task handler implementation and testing on the target 4. LED task and Button interrupt handling code implementation 5. Task Delete Implementation 6. Task Priority Implementation and testing 7. vTaskDelay() Implementation 8. Synchronizing a Task and Multiple Events 9. Mutual Exclusion between 2 tasks using Binary Semaphore					
<u>Lab Requirements:Software:</u>	1. FreeRTOS 2. Open STM32 System Work bench					

Hardware:	1. The development kits of ARM Developer Kits/ STM32F4 Discovery and Nucleo board. 2. Serial Cables, Network Cables and recommended power supply for the board.
E-resources and other digital material	1. https://training.ti.com/ti-rtos-workshop-series-1-10-welcome

Name of Course Coordinator :R V H Prasad**,** Assistant Professor

19ECVE2052: MIXED SIGNAL DESIGN LAB

Course Category:	Laboratory	**Credits:**	1.5
Course Type:	Practical	**Lecture - Tutorial -Practice:**	0-0-3
Prerequisites:	Analog and Mixed Signal IC Design	**Continuous Evaluation:** **Semester end Evaluation:** **Total Marks:**	40 60 100

Course Outcomes	Upon successful completion of the course, the student will be able to:					
	CO1	Design and analyze Analog and Mixed signal MOS circuits				
Contribution of Course Outcomes towards achievement of Program Outcomes (L – Low, M - Medium, H – High)		PO1	PO2	PO 3	PO 4	PO5
	CO1	H	L	M	M	
List of Experiments	**Design the following circuits with given specifications, completing the design flow mentioned below**: **Design the following circuits with given specifications, completing the design flow mentioned below**: (Minimum 10 Experiments) a. Design and perform the following analysis as per the requirement i. DC ii. Transient iii. Op iv. AC b. Draw the Layout and verify the DRC and LVS c. Extract RC and back annotate the same and verify the Design d. Verify & Optimize for Time, Power and Area to the given constraint 1. Inverter 2. Common source amplifier 3. Common gate amplifier 4. Common drain amplifier 5. Current mirror 6. MOS Differential amplifier 7. Operational amplifier 8. R-2R DAC 9. SAR based ADC 10. Ring Oscillator 11. Phase Locked Loop 12. Unity Gain Sampler					

Text books and Reference books	**Text Books:** 1. Jan M. Rabaey, Anantha P. Chandrakasan, BorivojeNikolic, (2011) "Digital Integrated Circuits: a Design Perspective", Pearson Education, 2nd Edition. 2. BehzadRazavi (2002), 'Design of Analog CMOS Integrated Circuits' Tata-McGrawHill.

Name of Course Coordinator: RajasekharTuraka