DETAILED

SYLLABUS

for

M Tech Degree Course

(Semester System)

VLSI DESIGN AND EMBEDDED SYSTEMS

w.e.f 2015-2016

COURSE STRUCTURE MTECH-15

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VELAGAPUDI RAMAKRISHNA

SIDDHARTHA ENGINEERING COLLEGE

(AUTONOMOUS)

(An Autonomous, ISO 9001:2008 Certified Institution)

(Approved by AICTE, Accredited by NAAC with 'A' Grade, Affiliated to JNTUK, Kakinada)

(Sponsored by Siddhartha Academy of General & Technical Education)

Kanuru, Vijayawada

Andhra Pradesh - 520007, INDIA.

www.vrsiddhartha.ac.in

W.E.F. 2015-16

MTECH-15

ACADEMIC REGULATIONS

MASTER OF TECHNOLOGY

(MTECH-15) w. e. f: 2015-2016

(Common to all branches)

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Academic Regulations for M. Tech (M.TECH-15) w. e. f: 2015-2016

(Common to all branches)

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1. INTRODUCTION

Academic Programmes of the College are governed by rules and regulations as approved by the Academic Council, which is the highest Academic Body of the Institute. These academic rules and regulations are effective from the academic year 2015-16, for students admitted into two year PG programme offered by the college leading to Master of Technology (M. Tech).

The regulations listed under this head are common for postgraduate programmes, leading to award of M. Tech degree, offered by the college with effect from the academic year 2015-16 and they are called as "M. TECH-15" regulations.

The regulations hereunder are subjected to amendments as may be made by the Academic Council of the college from time to time, keeping the recommendations of the Board of Studies in view. Any or all such amendments will be effective from such date and to such batches of candidates including those already undergoing the programme, as may be decided by the Academic Council.

2. DEFINITIONS

a) "Commission" means University Grants Commission (UGC)
b) "Council" means All India Council for Technical Education (AICTE)
c) "University" means Jawaharlal Nehru Technological University Kakinada, Kakinada (JNTUK)
d) "College" means Velagapudi Ramakrishna Siddhartha Engineering College (VRSEC)
e) "Programme" means any combination of courses and/or requirements leading to the award of a degree
f) "Course" means a subject either theory or practical identified by its course title and code number and which is normally studied in a semester.
g) "Degree" means an academic degree conferred by the university upon those who complete the postgraduate curriculum.

3. PROGRAMMES OFFERED

The nomenclature and its abbreviation given below shall continue to be used for the degree programmes under the University, as required by the Council and Commission.

Master of Technology (M. Tech) Besides, the name of the programme shall be indicated in brackets after the abbreviation. For example PG engineering degree in Computer Science and Engineering is abbreviated as M. Tech (Computer Science and Engineering).

Presently, the college is offering Post Graduate programme in Engineering with the following programmes:

Table 1: List of Programmes offered by college leading to M. Tech Degree

S. No	Programme	Department
1	Structural Engineering	Civil Engineering
2	Computer Science and Engineering	Computer Science and Engineering
3	Power Systems Engineering.	Electrical and Electronics Engineering
4	Communication Engineering and Signal Processing	Electronics and Communication Engineering
5	Telematics	
6	VLSI Design and Embedded Systems	
7	Computer Science & Technology	Information Technology
8	CADCAM	Mechanical Engineering
9	Thermal Engineering	

These Regulations shall be applicable to any new postgraduate programme (M. Tech) that may be introduced from time to time.

4. DURATION OF THE PROGRAMME

- The duration of the programme is two academic years consisting of four semesters.
- A student is permitted to complete the programme within a maximum duration of 4 years.

5. MINIMUM INSTRUCTION DAYS

- Each semester shall consist of a minimum of 90 instruction days with about 25 to 35 contact periods per week.

6. ELIGIBILITY CRITERIA FOR ADMISSION

- The eligibility criteria for admission into M.Tech programme are as per the guidelines of Andhra Pradesh State Council of Higher Education (APSCHE).

6.1 CATEGORY –A Seats:

- These seats will be filled by the Convener, PGECET Admissions.

6.2 CATEGORY –B Seats :

- These seats will be filled by the College as per the guidelines of Andhra Pradesh State Council of Higher Education (APSCHE).

7. PROGRAMME STRUCTURE

The programme structure is designed in such a way that it facilitates the courses required to attain the expected knowledge, skills and attitude by the time of their post-graduation as per the needs of the stakeholders. The curriculum structure consists of various course categories to cover the depth and breadth required for the programme and for the attainment of programme outcomes of the corresponding programme.

7.1 Programme Core:

The core consists of set of courses considered necessary for the students of the specific. The courses under this category should satisfy the programme specific criteria prescribed by the appropriate professional societies. The credits for programme core courses is 40.

7.2 Programme Electives:

The electives are set of courses offered in the which covers depth and breadth to further strengthen their knowledge. The students may register for appropriate electives offered in the based on their area of interest. The credits for the programme electives are 12.

7.3 Independent Learning:

The students are expected to learn the courses offered under this category on their own. The courses offered under this category include:

7.3.1 Self-Learning Course:

The self-learning courses shall be taken from the list of approved MOOCs in the respective Board of Studies. The courses under this category shall carry two credits.

7.3.2 Seminar:

One seminar shall be delivered by the students as individual presentation. The seminar topics shall be related to the contemporary aspects of the programme. The seminar shall carry 2 credits.

- The self learning course and seminar shall be offered either in 1st year or in 2nd year of the programme depending upon this scheme approved by BOS & Academic Council.

7.3.3 Project:

The Project shall be offered in 2nd year of the programme. The project shall be carried out by the students, as individual project, for a minimum period of one academic year. The project shall be carried out in the major areas pertaining to the programme approved by Project Review Committee and may address the societal problems/issues related to the programme. The project shall consist of Part-A and Part-B with a weightage of 10 and 14 credits, respectively spreading over for one semester each. The project part B shall be the extension of project Part A.

- If a candidate wishes to change his/her topic of the project, he/she can do so with approval of the project review committee within one week from the completion of 1st review.

7.3.3.1 PROJECT IN COLLABORATION WITH INDUSTRY:

- A student may, with the approval of the Head of the Department/Centre, visit an industry or a Research Laboratory for data collection, discussion of the project, experimental work, survey, field studies, etc. during the project period. Projects sponsored by the industry or Research Laboratories will be encouraged and a close liaison with such organizations will be maintained.
- A student may, with the approval of Project Review Committee, do the project work in collaboration with an industry, a Research and Development Organization. A Joint Supervisor may be appointed from the Industry and Research Laboratory with the approval of the HOD. The student shall acknowledge the involvement and / or contribution of an industry, R&D organization in completing the project in his/her thesis and a certificate to this effect, issued by the supervisor from the industrial organization, will be included in the thesis. The Internal Supervisor may visit the industry or the research laboratory in connection with the project work of his / her student if felt necessary.
- It is mandatory for all the students (especially those who do their project in an Industry, R&D organization in India or abroad) to make full disclosure of all data on which they wish to base their project. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. Any tangible intellectual property other than copyright

of the thesis may have to be assigned to the Institute. The copyright of the thesis itself would however lie with the student as per the IPR policy in force.

7.4 Course Code and Course Numbering Scheme

Course Code consists of Nine characters in which the one is the numeral and second to fourth are alphabets and the rest are numerals.

- The First character '15' indicates year of regulation.
- The second to fourth characters are described in Table 2 and 3.

Table 2: Second to Third Character description

Second & Third Characters	Name of the Department
CE	Civil Engineering Department
CS	Computer Science and Engineering Department
EC	Electronics & Communication Engineering Department
EE	Electrical & Electronics Engineering Department
IT	Information Technology Department
ME	Mechanical Engineering Department

The fourth and fifth characters represents specialization offering as mentioned in Table No. 3.

Table 3: Fourth and Fifth Character description

Fourth & Fifth Characters	Name of the Specialization
SE	Structural Engineering
CS	Computer Science and Engineering
SP	Communication Engineering and Signal Processing
VE	VLSI Design and Embedded Systems
TM	Telematics
PS	Power Systems Engineering
CT	Computer Science & Technology
CC	CADCAM
TE	Thermal Engineering

For all the Sixth and Seventh characters represent semester number and syllabus version number of the course offered.

Eighth character represents course type, as per Table No. 4

Table 4: Course type description

EIGHTH CHARACTER	DESCRIPTION
0	Theory course
5	Lab course

Nineth character represents course number as described in Figure 1 below.

For example, in **15 MECC 1051** course, the numeral **15** indicates year of regulation and the course is offered by Mechanical Engineering Department (**ME**) in CAD/CAM specialization offered in the first semester (**1**), the course syllabus version number (**0**), the course is of lab type (**5**) and the course number is (**1**), as given in figure.1 below.

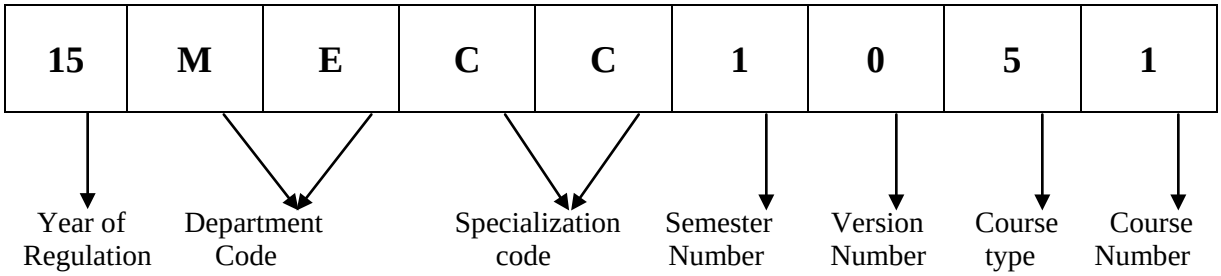

Figure 1: Course Code Description

7.5 Scheme of Instruction for 1st and 2nd Years

- The scheme of instruction and exact syllabi of all post graduate programmes are given separately.

7.6 Contact Hours and Credits

Credit means quantifying and recognizing learning. Credit is measured in terms of contact hours per week in a semester.

The Course Credits are broadly fixed based on the following norms:

- Lectures – One Lecture period per week is assigned one credit.
- Tutorials - Two tutorial periods per week are assigned one credit.
- Practical – 2 periods per week is assigned one credit
- Seminar/Mini Project shall have 2 credits.

- Major Project shall have 24 credits.
- However, some courses are prescribed with fixed number of credits depending on the subject complexity and importance.

7.7 Theory / Tutorial Classes

Each course is prescribed with fixed number of lecture periods per week. During lecture periods, the course instructor shall deal with the concepts of the course. For certain courses, tutorial periods are prescribed, to give exercises to the students and to closely monitor their learning ability.

7.8 Laboratory Courses

A minimum prescribed number of experiments have to be performed by the students, who shall complete these in all respects and get each experiment evaluated by teacher concerned and certified by the Head of the Department concerned at the end of the semester.

7.9 Programme Credits

Each specialization of M. Tech programme is designed to have a total of 80 credits, and the student shall have to earn all the credits for the award of degree.

8. MEDIUM OF INSTRUCTION

The medium of instruction and examination is English.

9. SYLLABUS

As approved by the concerned BOS and the Academic Council.

10. ELIGIBILITY REQUIREMENT FOR APPEARING SEMESTER END EXAMINATION AND CONDONATION

- A regular course of study means a minimum average attendance of 75% in all the courses computed by totaling the number of periods of lectures, tutorials, practical courses and project as the case may be, held in every course as the denominator and the total number of periods attended by the student in all the courses put together as the numerator.
- Condonation of shortage in attendance may be recommended by the respective Heads of Departments on genuine medical grounds, provided the student puts in at least 65% attendance as calculated above and provided the Principal is satisfied with the genuineness of the reasons and the conduct of the student.

- Students, having shortage of attendance, shall have to pay the requisite fee towards condonation**.**
- Minimum of 50% aggregate marks must be secured by the candidates in the continuous evaluations conducted in that semester for courses such as theory, laboratory courses, seminar and project to be eligible to write semester end examinations. However, if the student is eligible for promotion based on the attendance, in case necessary, a shortage of internal marks up to a maximum of 10% may be condoned by the Principal based on the recommendations of the Heads of the Departments.
- Students having shortage of internal marks up to a maximum of 10% shall have to pay requisite fee towards condonation**.**
- A student, who does not satisfy the attendance and/or internal marks requirement, shall have to repeat that semester.
- Eligible candidates who failed to register for all courses for the semester-end examinations shall not be permitted to continue the subsequent semester and has to repeat the semester for which he/she has not registered for semester end examinations.

11. EXAMINATIONS AND SCHEME OF EVALUATION

11.1 Continuous Evaluation:

11.1.1 Theory Courses

Each course is evaluated for **40** marks (a+b)

a) The continuous evaluation shall be made based on the two midterm examinations each of 2**0** marks will be conducted in every theory course in a semester. The mid term marks shall be awarded giving a weightage of $2/3^{rd}$ in the examination in which the student scores more marks and $1/3^{rd}$ for the examination in which the student scores less marks. Each midterm examination shall be conducted for duration of 90 minutes without any choice**.**

b) The remaining 20 marks are awarded through continuous evaluation of assignments / mini project in each subject as notified by the teacher at the beginning of the semester.

Students shall be informed regarding the comprehensive assignment/ during the first week of the semester and they have to submit completed assignment on or before 12^{th} week of semester.

11.1.2 Laboratory Courses: 40 marks

- For Laboratory courses there shall be continuous evaluation during the semester for 40 continuous evaluation marks. The distribution of continues evaluation marks is given below:

Table 5: Distribution of Marks

Sl. No.	Criteria	Marks
1	Day to Day work	10
2	Record	10
3	Continuous Evaluation	20

11.1.3 Seminar: 40 marks

The distribution of continues evaluation marks for the seminar is given below.

Table 6: Distribution of Marks

Sl. No.	Criteria	Marks
1	Report	15
2	Presentation	15
3	Viva-voce	10

The Seminar Review Committee (SRC) to be constituted by HOD with minimum two members related to programs specialization.

11.1.4 Project: (40 marks)

The continuous evaluation (Project Part A and Project Part B) for 40 marks shall be on the basis of two seminars by each student evaluated by a review committee and the day to day assessment by the supervisor in respective semester. The review committee consists of HOD, Programme coordinator, respective internal guide and two senior members of faculty of the department with expertise in the respective specialization nominated by HOD. The distribution of marks is as follows in Table 7.

Table 7: Continuous evaluation in each semester

Sl. No.	Criteria	Marks
1	Two reviews	15+15
2	Day to day assessment	10

Rubrics shall be prepared by review committee using appropriate performance indicators for each review separately and informed to the students well in advance.

11.1.5 Self-Learning Courses

For the courses under this category, there shall be continuous evaluation for 40 marks and semester end examination of 60 marks. The distribution of marks for continuous evaluation will be same as theory courses (Section 11.1.1).

11.2 SEMESTER END EXAMINATIONS

11.2.1 Theory Courses: 60 marks

The Semester end examinations shall be conducted for 3 hours duration at the end of the semester. The question paper shall be given in the following pattern: There shall be two questions from each unit with internal choice. Each question carries 15 marks. Each course shall consist of four units of the syllabus.

11.2.2 Lab Courses: 60 marks

40 marks are allotted for experiments/job works & **15** marks are allotted for viva-voce examination and **5** marks for the record.

11.2.3 Seminar: 60 marks

There shall be a seminar presentation. For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department, supervisor and two other senior faculty members of the department. For Seminar, the evaluation is done for 60 marks internally.

11.2.4 Self-Learning Courses: 60 marks

The semester end examinations for courses under this category are evaluated for 60 marks.

11.2.5 Project: 60 marks

The project (Project Part A and Part B) shall be evaluated for 60 marks in respective semesters. The semester end examination for project part – A shall be evaluated by HOD, Programme coordinator and one of the senior Professors of the Department.

Project part – B shall be evaluated by a project evaluation committee consisting of the Head of the Department, project internal guide and an external examiner approved by the Principal from a panel submitted by the HOD.

The rubrics for evaluation of semester end examination shall be defined by the Project review committee separately for Part – A and Part B.

12. CONDITIONS FOR PASS AND AWARD OF CREDITS FOR A COURSE

12.1 Conditions for Pass and award of Grades & Credits:

a) A candidate shall be declared to have passed in individual Theory course if he/she secures a minimum of 50% aggregate marks (continues evaluation & semester end examination marks put together), subject to a minimum of 40% marks in the semester end examination.

b) A candidate shall be declared to have passed in individual labs/ seminar/ course if he/she secures a minimum of 50% aggregate marks (continues evaluation & semester end examination marks put together), subject to a minimum of 50% marks in the semester end examination.

c) If a candidate secures minimum of 40% marks in Theory Courses in the semester end examination and 40% - 49% of the total marks in the semester end examination and continues evaluation taken together in some theory courses and secures an overall aggregate of 50% in all theory courses in that semester he/she declared to be passed in the theory courses of that semester in semester end Examinations. This provision is applicable for Regular candidates only during Regular Semester – end Examinations.

d) The student has to pass the failed course by appearing the examination when conducted subsequently, as per the requirement for the award of degree.

e) A candidate shall be declared to have passed the Project part A/ **P**roject part B, if he/she secures minimum of 50 % aggregate marks (continuous evaluation and semester end examination marks put together), subject to a minimum of 50 % of marks in semester end examinations.

f) If any candidate does not fulfill the pass requirement as per 12.1.(e) in semester end examination of Project Part – A, he / she will be given two months additional time to

re appear at the semester end examination after paying the requisite examination fee and also the candidate has to bear the expenditure for conducting examination. If the candidate does not fulfill the pass requirement again in Project Part – A as per 12.1(e), he/she has to repeat the semester in next academic year.

g) In a special case, if any student does not submit his / her thesis of Project Part – B, due to ill health or any other genuine reason, he / she will be given another chance to appear at Project Part - B examination conducted separately at a later date i.e. within two months from the completion of Project Part – B semester end examination of that particular academic year after paying the requisite examination fee, if the expenditure for conducting Project Part – B is completely borne by the candidate.

h) On passing a course of a programme, the student shall earn assigned credits in that Course.

12.2 Method of Awarding Letter Grades and Grade Points for a Course.

A letter grade and grade points will be awarded to a student in each course based on his/her performance as per the grading system given below.

Table 8: Grading System for individual subjects/labs

Theory	Lab	Grade Points	Letter Grade
>= 90%	>= 90%	10	Ex
80-89%	80-89%	9	A+
70-79%	70-79%	8	A
60-69%	60-69%	7	B
50-59%	55-59%	6	C
45-49%	50-54%	5	D
40-44%	-	4	E
< 40%	< 50%	0	F (Fail)
ABSENT	ABSENT	0	AB

12.3 Calculation of Semester Grade Points Average (SGPA)* and award of division for the program.

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as below:

$$SGPA = \frac{\sum(CR \times GP)}{\sum CR}$$ (For all courses passed in semester)

Where CR= Credits of a course

GP = Grade points awarded for a course

*SGPA is calculated for the candidates who passed all the courses in that semester.

12.4 Calculation of Cumulative Grade Point Average (CGPA) for Entire Programme.

The CGPA is calculated as below:

$$CGPA = \frac{\sum(CR \times GP)}{\sum CR}$$ (For entire programme)

Where CR= Credits of a course

GP = Grade points awarded for a course

Table 9: Award of Divisions

CGPA	DIVISION
≥7.75	First Class with distinction
≥6.5 - <7.75	First Class
≥5.5 - <6.5	Second Class
≥4 - <5.5	Pass Class
<4	Fail

For the purpose of awarding first class with distinction, the candidate should complete the programme with in 2 years and should get required CGPA.

Detained, Break in study candidates, and the candidates who availed themselves of the opportunity of extension of project part – B for a further period of two months are not eligible for the award of first class with distinction.

For the purpose of awarding first/ second/ pass class, CGPA obtained in the examinations appeared within the maximum period allowed for the completion of course including extensions in project, if any shall be considered.

12.5 Transitory Regulations

A candidate, who is detained or discontinued in the semester, on readmission shall be required to pass all the courses in the curriculum prescribed for such

batch of students in which the student joins subsequently and the academic regulations be applicable to him/her which have in force at the time of his/her admission. However, exemption will be given to those candidates who have already passed in such courses in the earlier semester(s) and additional subjects are to be studied as approved by Board of Studies and ratified by Academic Council.

12.6 Consolidated Grade Card

A consolidated grade card containing credits & grades obtained by the candidates will be issued after completion of the two years M. Tech Programme.

13.READMISSION CRITERIA

A candidate, who is detained in a semester due to lack of attendance/marks, has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling all the required norms stipulated by the college in addition to paying an administrative fee of Rs. 1,000/-.

Rules for Calculation of Attendance for Re- Admitted students.

a) No.of classes conducted will be counted from the day 1 of the semester concerned, irrespective of the date of payment of tuition fee.
b) They should submit a written request to the principal of the college, along with a challan paid towards tuition and other fee. for re – admission before the commencement of class work.
c) Student should come to know about the date of commencement of class – work of the semester in to which he / she wishes to get re – admission. The information regarding date of commencement of class – work for each semester is available in the college notice boards / website.

14. BREAK IN STUDY

Student, who discontinues the studies for whatsoever may be the reason, can get readmission into an appropriate semester of M. Tech program after a break-in study only with the prior permission of the Principal of the College provided such candidate shall follow the transitory regulations applicable to such batch in which he/she joins. An

administrative fee of Rs. 2000/- per each year of break in study in addition to the prescribed tuition and special fee has to be paid by the candidate to condone his/her break in study.

15. ELIGIBILITY FOR AWARD OF M.TECH. DEGREE

The M. Tech., Degree shall be conferred on a candidate who satisfies the following requirement. A student should register himself for 80 Credits, and should obtain all the 80 credits in order to become eligible for the award of M.Tech Degree.

16. CONDUCT AND DISCIPLINE

- Students shall conduct themselves within and outside the premises of the Institute in a manner befitting the students of our Institute.
- As per the order of the Honorable Supreme Court of India, ragging in any form is considered a criminal offense and is banned. Any form of ragging will be severely dealt with.
- The following acts of omission and/or commission shall constitute gross violation of the code of conduct and are liable to invoke disciplinary measures with regard to ragging.

i. Lack of courtesy and decorum; indecent behavior anywhere within or outside the campus.

ii. Willful damage or distribution of alcoholic drinks or any kind of narcotics to fellow students /citizens.

The following activities are not allowed within the campus

- Possession, consumption or distribution of alcoholic drinks or any kind of narcotics or hallucinogenic drugs.
- Mutilation or unauthorized possession of library books.
- Noisy and unseemly behavior, disturbing studies of fellow students.
- Hacking computer systems (such as entering into other person's areas without prior permission, manipulation and/or damage of computer hardware and software or any other cyber crime etc.
- Use of cell phones in the campus.
- Plagiarism of any nature.
- Any other act of gross indiscipline as decided by the college from time to time.
- Commensurate with the gravity of an offense, the punishment may be reprimanded, fine, expulsion from the institute / hostel, debarment from a examination, disallowing the use of

certain facilities of the Institute, rustication for a specified period or even outright expulsion from the Institute, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.

- For an offense committed in (i) a hostel (ii) a department or in a classroom and (iii) elsewhere, the Chief Warden, the Head of the Department and the Principal, respectively, shall have the authority to reprimand or impose fine.
- Cases of adoption of unfair means and/or any malpractice in an examination shall be reported to the Principal for taking appropriate action.
- Unauthorized collection of money in any form is strictly prohibited.
- Detained and Break-in-Study candidates are allowed into the campus for academic purposes only with permission from the authorities.
- Misconduct committed by a student outside the college campus, but having the effect of damaging, undermining & tarnishing the image & reputation of the institution will make the student concerned liable for disciplinary action commensurate with the nature & gravity of such misconduct.
- The Disciplinary Action Committee constituted by the Principal, shall be the authority to investigate the details of the offense, and recommend disciplinary action based on the nature and extent of the offense committed.
- "Grievance appeal Committee" (General) constituted by the Principal shall deal with all grievances pertaining to the academic / administrative /disciplinary matters.
- All the students must abide by the code and conduct rules of the college.

17. MALPRACTICES

- The Principal shall refer the cases of malpractices in internal assessment tests and Semester-End Examinations, to a Malpractice Enquiry Committee, constituted by him/her for the purpose. Such committee shall follow the approved scales of punishment. The Principal shall take necessary action, against the erring students based on the recommendations of the committee.
- Any action on the part of the candidate at an examination trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder. The involvement of the Staff, who are in charge of conducting examinations, valuing examination papers and preparing/keeping records of documents relating to the examinations in such acts (inclusive

of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.

18. OTHER MATTERS

18.1 The physically challenged candidates who have availed additional examination time and a scribe during their B. Tech/PGECET/GATE examinations will be given similar concessions on production of relevant proof/documents.

18.2 Students who are suffering from contagious diseases are not allowed to appear either internal or semester end examinations.

18.3 The students who participated in coaching/tournaments held at the state / National /International levels through University / Indian Olympic Association during the end semester external examination period will be promoted to subsequent semesters till the entire course is completed as per the guidelines of University Grants Commission Letter No. F.1-5/88 (SPE/PES), dated 18-08-1994.

18.4 The Principal shall deal with any academic problem, which is not covered under these rules and regulations, in consultation with the Heads of the Departments in an appropriate manner, and subsequently such actions shall be placed before the academic council for ratification. Any emergency modification of regulation, approved in the Heads of the Departments Meetings, shall be reported to the academic council for ratification.

19. AMENDMENTS TO REGULATIONS

The Academic Council may, from time to time, revise, amend, or change the regulations, Schemes of examination and/or syllabi.

ELECTRONICS AND COMMUNICATION ENGINEERING
Curriculum, Scheme of Examination and Syllabi
For M.Tech Degree Program
in
VLSI Design & Embedded Systems
being offered at
Velagapudi Ramakrishna Siddhartha EngineeringCollege
w.e.f 2015-2016
FIRST SEMESTER

Code	Subject	L	P	C	I	E	T
15ECVE1001	Principles of Embedded Systems	4	0	4	40	60	100
15ECVE1002	Advanced Digital Design using Verilog HDL	4	0	4	40	60	100
15ECVE1003	CMOS Digital IC Design	4	0	4	40	60	100
15ECVE1004	Microcontrollers for Embedded Systems	4	0	4	40	60	100
15ECVE1005/1	Semiconductor Device Modeling	3	0	3	40	60	100
15ECVE1005/2	Fabrication Technology						
15ECVE1005/3	Embedded Hardware Design						
15ECVE1005/4	Advanced Computer Architecture						
15ECVE1006/1	Embedded Software Design	3	0	3	40	60	100
15ECVE1006/2	CPLD and FPGA Architectures						
15ECVE1006/3	High Speed Digital Design						
15ECVE1006/4	System on Chip						
15ECVE1051	VLSI Design Lab	0	3	2	40	60	100
15ECVE1052	Embedded System Lab	0	3	2	40	60	100
	Total Credits (6 Theory + 2 Labs)	22	06	26	320	480	800

L: Lecture **P**: Practice **C**: Credits

I: Internal Assessment **E**: End Examination **T**: Total Marks

ELECTRONICS AND COMMUNICATION ENGINEERING
Curriculum, Scheme of Examination and Syllabi
For M.Tech Degree Program
in
VLSI Design & Embedded Systems
being offered at
Velagapudi Ramakrishna Siddhartha EngineeringCollege
w.e.f 2015-2016
SECOND SEMESTER

Code	Subject	L	P	C	I	E	T
15ECVE2001	Low Power VLSI Design	4	0	4	40	60	100
15ECVE2002	Analog and Mixed Signal Design	4	0	4	40	60	100
15ECVE2003	Embedded Device Drivers	4	0	4	40	60	100
15ECVE2004	Real Time Operating Systems	4	0	4	40	60	100
15ECVE2005/1	Testing and Testability	3	0	3	40	60	100
15ECVE2005/2	Embedded System Design						
15ECVE2005/3	Real Time Systems						
15ECVE2005/4	Physical Design Automation						
15ECVE2006/1	Hardware software co-design	3	0	3	40	60	100
15ECVE2006/2	Embedded Networking						
15ECVE2006/3	VLSI Signal Processing						
15ECVE2006/4	PERL Scripting Language						
15ECVE2051	Analog & Digital IC Lab	0	3	2	40	60	100
15ECVE2052	Embedded System Design Lab	0	3	2	40	60	100
	Total Credits (6 Theory + 2 Lab)	22	06	26	320	480	800

L: Lecture **P**: Practice **C**: Credits

I: Internal Assessment **E**: End Examination **T**: Total Marks

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THIRD SEMESTER

Code	Subject	L	P	C	I	E	T
	MOOCS						
15ECVE3001/1	Fundamentals of Nanoelectronics						
15ECVE3001/2	Linux Programming and Scripting	0	0	2	40	60	100
15ECVE3001/3	RF Integrated Circuits						
15ECVE3001/4	Embedded Software Testing						
15ECVE3051	Project work – Part A	0	0	10	40	60	100
15ECVE3052	Seminar	0	0	2	40	60	100
	Total	0	0	14	120	180	300

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FOURTH SEMESTER

Code	Subject	L	P	C	I	E	T
15ECVE4051	Project work–Part B	0	0	14	40	60	100

15ECVE1001

PRINCIPLES OF EMBEDDED SYSTEMS

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes

Upon completion of the course student will be able to

1. Recognize the basic building blocks and components of embedded systems and microcontroller.
2. Recognize and define the categories, properties, features, design criteria and example hardware of embedded systems.
3. Define and design digital systems and circuits of embedded systems, differentiate the properties of embedded systems and microcomputers.
4. Recognize the design requirements from user perspective, and relate them to real time operating systems.

UNIT I

Introduction - Introduction to embedded systems: Overview, Common Design Metrics, Processor Technology, IC technology, Design technology, Trade-offs, Custom Single-Purpose Processors: Hardware, Combinational logic, Sequential logic, Custom single-purpose processor design, Optimization of Custom single-purpose processors.

UNIT II

General-Purpose Processors - Software, Basic Architecture, Operation, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPs), General-Purpose Processor Design.

Standard Single-Purpose Processors - Peripherals, UART, Pulse Width Modulators, LCD, Keypad and Stepper Motor Controllers, Analog-to-Digital Converters, Real-Time Clocks.

UNIT III

Memory - common memory types, Advanced RAM, Interfacing: Terminology and Basic Protocol Concepts, Microprocessor Interfacing: Interrupts, Direct Memory Access, Arbitration. Multi level bus architectures.

UNIT IV

Digital Camera Example - User's and Designer's perspective, Requirements specification, Design.

Introduction to Real Time Operating Systems - OS and RTOS basics**,** Real time operating system architecture.

Text Books

1. Frank Vahid, Tony Givargis (2005), “Embedded System Design”, J Wiley India.
2. David Simon (1999), “An Embedded Software Primer”, Pearson Education.

Reference Books

1. K V K K Prasad, “Embedded Real Time Systems: Concepts, Design Programming”, Dreamtech Press.
2. Wayne Wolf (2012), “Computers as Components: Principles of Embedded Computing System Design”, 3rd Ed, Morgan Kaufmann publishers.

15ECVE1002

ADVANCED DIGITAL DESIGN USING VERILOG HDL

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes:

Upon the completion of this course, students will be able to

1. Design and synthesize combinational and sequential logic.
2. Develop architectures for processors and controllers.
3. Apply post synthesis design tasks for any design.

UNIT I

Introduction to Digital Design Methodology - Glitches and Hazards, Design of sequential machines, state-transition graphs, design example: BCD to Excess-3 code converter, serial - line code converter for data transmission, state reduction, and equivalent states, Algorithmic State Machine Charts for behavioral modeling, ASMD charts, switch debounce, metastability, and synchronizers for asynchronous signals, design example: keypad scanner and encoder.

UNIT II

Synthesis of Combinational and Sequential Logic - Introduction to synthesis, synthesis of combinational logic, synthesis of sequential logic with flip-flops, synthesis of explicit state machines, registered logic, state encoding, synthesis of implicit state machines, registers, and counters, synthesis of gated clocks and clock enables

UNIT III

Design and Synthesis of Datapath Controllers - Partitioned sequential machines, design example: binary counter, design and synthesis of a RISC stored-program machine, design example: UART

Algorithms and Architecture for Digital Processors - Algorithms, nested-loop programs, and data flow graphs, digital filters and signal processors, building blocks for signal processors, asynchronous FIFOs- synchronization across clock domains.

UNIT IV

Post synthesis Design Tasks - Post synthesis design validation, post synthesis timing verification, estimation of ASIC timing violations, false paths, system tasks for timing verification.

Text Books

1. Michael D. Ciletti (2002), “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

Reference Books:

1. Stephen Brown & Zvonko Vranesic (2007) , ”Fundamentals of Digital logic with Verilog design”, 2nd edition, Tata McGraw Hill,.
2. Ian Grout (2011), “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.
3. Palnitkar, S. (2003). Verilog HDL: a guide to digital design and synthesis (Vol. 1). Prentice Hall Professional.

15ECVE1003

CMOS DIGITAL IC DESIGN

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes:

Upon the completion of this course, students will be able to

1. Evaluate the performance of CMOS Inverter in terms of area, power and speed.
2. Evaluate the performance and power consumption of contemporary gate logic families
3. Analyze and apply timing issues for designing sequential circuits.

UNIT I

The CMOS Inverter - Static CMOS Inverter, Static Behaviour, Performance of CMOS Inverter: Dynamic Behaviour, Power, Energy, and Energy- Delay, Technology Scaling and its Impacts on the Inverter Metrics.

UNIT II

Designing Combinational Logic Gates in CMOS - Static CMOS Design – Complementary CMOS, Ratioed Logic, Pass Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principle, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates.

UNIT III

Designing Sequential Logic Circuits - Introduction, Static Latches and Registers, Dynamic Latches and Registers, Pipelining: An approach to Optimize Sequential Circuits, Non-Bistable Sequential Circuits, Choosing a Clocking Strategy.

UNIT IV

Timing Issues in Digital Circuits - Timing Classification of Digital Systems, Synchronous Interconnect, Synchronous Design, Clock Synthesis and Synchronization using a Phase Locked Loop, Future Directions and Perspectives.

Text Books

1. Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolic, (2003) “Digital Integrated Circuits: a Design Perspective”, 2nd Edition, Pearson Education.

Reference Books

1. J. Uyemura (1992), Circuit Design for CMOS VLSI, Kluwer.
2. Kang and Leblebici, (1999) CMOS Digital Integrated Circuits, 2nd Ed., McGraw-Hill.

15ECVE1004

MICROCONTROLLERS FOR EMBEDDED SYSTEMS

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course outcomes:

Upon completion of the course students will be able to

1. Understand and analyze the design aspects, Architecture, and instruction set associated with ARM processors.
2. Analyze the C programming optimization methods for ARM processor
3. Examines various cache-technologies that surround the ARM cores.

UNIT I

ARM Architecture - ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT II

ARM Programming Model-I - Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT III

ARM Programming Model-II - Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT IV

ARM Programming - Simple C Programs usingFunction Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, ConditionalExecution and Loops.

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

Text Books

1. A.Sloss, D.Symes, C.Wright, (2003), “ARM system Developers Guide: Designing and Optimizing System Software”, Morgan Kaufmann publishers.

Reference Books

1. Valvano, J. (2011),”Embedded microcomputer systems: real time interfacing”, 3rd Edition, Cengage Learning.

15ECVE1005/1

SEMICONDUCTOR DEVICE MODELING

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand the concepts of semiconductor device physics.
2. Analyze the BJT and MOSFET device characteristics
3. Understand the second order effects of BJT and MOSFET.

UNIT I

Energy bands in solids, Electrons and holes densities in equilibrium, Excess carriers - Non-equilibrium situation, Mobility of carriers, Charge transport in semiconductors, Continuity equation.

UNIT II

Introduction to BJT, Operation of BJT at high frequencies, Design of high frequency transistors, Second order effects in BJTs, Variation of beta with collector current, High injection in collector, Heavy doping in emitter, Non-conventional BJTs, Hetero-junction bipolar BJTs.

UNIT III

Metal-semiconductor junction, Energy band diagram of M-S junction, Current-voltage characteristics of M-S junction, Ohmic contacts, Junction field effect transistor, Small signal parameters of JFETs, The MESFETs, The Hetero- junction FETs.

UNIT IV

Introduction to MOSFETs, Effect of gate and drain voltages on carrier mobility in the inversion layer, Channel length modulation, MOSFET break down and punch-through, Sub-threshold current, MOSFET scaling, Non-uniform doping in channel, Threshold voltage of short channel MOSFETs, Small signal analysis, Other MOSFETs configuration.

Text Books

1. Nandita Das Guptha , Amitava Das Guptha (2004), “Semiconductor Devices Modelling and Technology”, Prentice Hall India

Reference Books

1. Ben G. Streetman (2000), “Solid State Electronic Devices”, 5th edition, Pearson Education Asia.

15ECVE1005/2

FABRICATION TECHNOLOGY

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon completion of the course students will be able to

1. Describe various fabrication steps involved in IC fabrication.
2. Understand the process of crystal growth, wafer preparation, epitaxial growth.
3. Understand significance of thin and thick oxidation in fabrication process.
4. Understand the development of metallic interconnects through lithography, metallization, etching.

UNIT I

Crystal Growth and Wafer Preparation – Introduction, Electronic grade silicon, Czochralski crystal growing, Silicon shaping, Processing considerations.

Epitaxy – Introduction, Vapor phase epitaxy, Molecular beam epitaxy, Silicon-on-insulators, Epitaxial evaluation.

UNIT II

Oxidation – Introduction, Growth mechanism and kinetics, Thin oxides, Oxidation techniques and systems, Oxide properties, Redistribution of dopants at interface, Oxidation of polysilicon, Oxidation induced defects.

Lithography – Introduction, Optical lithography, Electron lithography, X-Ray lithography, Ion lithography.

Reactive Plasma Etching – Introduction, Plasma properties, Feature size control and anisotropic etch mechanisms, Reactive plasma etching techniques and equipment.

UNIT III

Dielectric and Polysilicon Film Deposition – Introduction, Deposition processes, Polysilicon, Silicon dioxide, Silicon nitride, Plasma assisted depositions.

Diffusion – Introduction, Models of diffusion in solids, Measurement techniques, Diffusion in polycrystalline silicon, Diffusion in SiO2.

UNIT IV

Ion Implantation – Introduction, Range theory, Implantation equipment, Annealing, Shallow junctions, High-energy implantation.

Metallization – Introduction, Metallization applications, Metallization choices, Physical vapor deposition, Patterning.

Text Books

1. S.M.Sze (2001), “VLSI Technology”, 2/E Tata McGraw-Hill.

Reference Books

1. Yasuo Tarui (1986),” VLSI Technology: Fundamentals and Applications”, Springer-Verlag.
2. Plummer (2001), “Silicon VLSI Technology: Fundamentals, Practice, and Modeling”, Pearson Education India.
3. S. K. Ghandhi, (1983), “VLSI Fabrication Principles: Silicon and Gallium Arsenide” Wiley, New York,
4. C.Y. Chang and S.M.Sze (Ed), (1996), “ULSI Technology”, McGraw Hill Companies Inc.
5. Stephen Campbell (1996), “The Science and Engineering of Microelectronics”, Oxford University Press,.

15ECVE1005/3

EMBEDDED HARDWARE DESIGN

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course outcomes:

Upon completion of the course, the student will be able to

1. Describe the 8051 architecture with various addressing modes.
2. Get familiar with the various memory technologies and interface the same to microcontroller.
3. Perform worst-case timing analysis for interfacing hardware to microcontroller.
4. Analyze CPU bus Cycles and Interface I/O devices to 8051.

UNIT I

Microcontroller Concepts: Organization, The 8051 Family Microcontroller Processor Architecture, Instruction Set Summary, Direct and Register Addressing, Indirect Addressing, Immediate Addressing, Generic Address Modes and Instruction Formats, Address Modes, The Software Development Cycle, Software Development Tools, Hardware Development Tools.

UNIT II

Worst - Case Timing, Loading, Analysis and Design: Timing Diagram Notation Conventions,Fan-Out and Loading Analysis DC and AC, Logic Family IC Characteristics and Interfacing, Design Example: Noise Margin Analysis Spreadsheet, Worst-Case Timing Analysis Example.

Memory Technologies and Interfacing: Memory Taxonomy, Read/Write Memories, Read-Only Memory, Other Memory Types, JEDEC Memory Pin-Outs, Device Programmers, Memory Organization Considerations, Parametric Considerations, Asynchronous vs Synchronous Memory, Error Detection and Correction, Memory Management, Read and Write Operations.

UNIT III

CPU Bus Interface and Timing: Address, Data, and Control Buses, Address Spaces and Decoding, Address Map, The Central Processing Unit (CPU).

A Detailed Design Example: External Data Memory Cycles, Design Problem 1, Design Problem 2, Design Problem 3, Memory Selection and Interfacing, Preliminary Timing Analysis.

UNIT IV

Basic I/O Interfaces: Port I/O for the 8051 Family, Output Current Limitations, Simple Input/output Devices, Program-Controlled I/O Bus Interfacing, Direct Memory Access (DMA), Elementary I/O Devices and Applications.

Other Interfaces and Bus Cycles: Interrupt Cycles, Software Interrupts, Hardware Interrupts.

Text Books

1. Arnold, K. (2001). Embedded controller hardware design. Newnes.

Reference Books

1. Williams, T. (2004). The circuit designer's companion. Butterworth-Heinemann, 2nd Edition
2. Catsoulis, J. (2005). Designing embedded hardware. O'Reilly Media, Inc
3. Ganssle, J., Noergaard, T., Eady, F., Edwards, L., Katz, D. J., Gentile, R., & Perrin, B. (2007). Embedded Hardware: Know It All: Know It All. Newnes..

15ECVE1005/4

ADVANCED COMPUTER ARCHITECTURE

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Describe quantitative evaluation of multi-threading.
2. Survey the limitations of Instruction-Level parallelism & Thread-level parallelism.
3. Understand the optimization techniques of cache performance.

UNIT I

Fundamentals of Computer design – Introduction, computing and task of computer designer, technology trends, cost, price and their trends, measuring and reporting performance, quantitative principles of computer design, power consumption and efficiency.

Instruction-Level parallelism and its exploitation - concepts and challenges, basic compiler techniques for exposing ILP reducing branch costs with prediction, overcoming data hazards with dynamic scheduling, Dunamic scheduling: examples and algorithm, hardware based speculation, exploiting ILP using multiple issue and static scheduling, exploiting ILP using dynamic scheduling, multiple issue, and speculation, advanced techniques for instruction delivery and speculation.

UNIT II

Limitations on instruction Level parallelism - Introduction, studies of the limitations of ILP, limitation on ILP for realizable processors, crosscutting issues: hardware versus software speculation, multithreading: using ILP support to exploit thread – level parallelism.

Multiprocessors and thread level parallelism - Introduction, symmetric shared memory architectures, performance of symmetric shared memory multiprocessors, distributed shared memory and directory based coherence, synchronization: the basics, models of memory consistency: an introduction, crosscutting issues.

UNIT III

Memory hierarchy design - Introduction, eleven advanced optimization of cache performance, memory technology and optimizations, protection: virtual memory and virtual machines, the design of memory hierarchies.

UNIT IV

Storage systems - Introduction, advanced topics in disk storage, definition and examples of real faults and failures, I/O performance, reliability measures and benchmarks, a little queuing theory, crosscutting issues, designing and evaluating an I/O system.

Text Books

1. L. Hennessy & David A. Patterson (2011) "Computer Architecture A quantitative approach" 4th edition, Morgan Kufmann (An Imprint of Elsevier).

Reference Books

1. Kai Hwang and A.Briggs (1984) "Computer Architecture and parallel Processing" International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk (1997), "Advanced Computer Architectures", Pearson.

15ECVE1006/1

EMBEDDED SOFTWARE DESIGN

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon completion of the course students will be able to

1. Illustrate linux programming concepts and embedded board support package.
2. Understand concepts of embedded storage and device drivers
3. Understand fundamentals of porting, building and debugging an embedded application
4. Use and get acquaint to embedded graphics.

UNIT I

Introduction-Why Embedded Linux?, Embedded Linux Versus Desktop, Embedded Linux Distributions, Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross-Platform Toolchain,

Board Support Package- Inserting BSP in Kernel Build Procedure, The Boot Loader Interface, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART , Power Management,

UNIT II

Embedded Storage- Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices, Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory

Embedded Drivers- Linux Serial Driver, Ethernet Driver, I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules,

UNIT III

Porting Applications- Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver

Building and Debugging- Building the Kernel, Building Applications, Building the Root File System, Integrated Development Environment, Debugging Virtual Memory Problems, Kernel Debuggers, Profiling,

UNIT IV

Embedded Graphics- Graphics System, Linux Desktop Graphics—The X Graphics System, Introduction to Display Hardware, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications

Text Books

1. Raghavan, P., Lad, A., & Neelakandan, S. (2005). Embedded Linux system design and development. CRC press.

Reference Books

1. Barr, M., & Massa, A. (2006). Programming embedded systems: with C and GNU development tools., O'Reilly Media, Inc.

15ECVE1006/2

CPLD AND FPGA ARCHITECURES

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of this course, students will be able to

1. Examine various programmable logic devices.
2. Comprehend FPGA programming technologies
3. Design applications using FPGA devices.

UNIT I

Introduction to Programmable Logic Devices - Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II

Field Programmable Gate Arrays - Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III

SRAM Programmable FPGAs - Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

Anti-Fuse Programmed FPGAs - Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT4Architectures.

UNIT IV

Design Applications - General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

15ECVE1006/3

HIGH SPEED DIGITAL DESIGN

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand the interconnect characteristics.
2. Apply the design concepts to power distribution network and signaling circuits.
3. Understand the timing and synchronization of clock signals.

UNIT I

Modeling and Analysis of Wires - Geometry and Electrical Properties of Resistance, Capacitance and Inductance, Electrical Models of Wires, Simple Transmission lines - Lossless LC Transmission Lines, Lossy LRC Transmission lines, Special Transmission lines.

UNIT II

Power Distribution - Power Supply Network - Local Regulation - IR Drops - Area Bonding – On-chip Bypass Capacitors - Symbiotic Bypass Capacitors - Power Supply Isolation, Noise Sources In Digital System - Power Supply Noise - Cross Talk - Intersymbol Interference.

UNIT III

Signaling Convention and Circuits - Signaling Modes for Transmission Lines -Signaling Over Lumped Transmission Media - Signaling Over RC Interconnect - Driving Lossy LC Lines - Simultaneous Bi-Directional Signaling, Terminations, Transmitter and Receiver Circuits.

UNIT IV

Timing Convention And Synchronization - Timing Fundamentals - Timing Properties of Clocked Storage Elements – Encoding Timings: Signals and Events, Open Loop Timing - Level Sensitive Clocking, Pipeline Timing. Closed Loop Timing, Clock Distribution, Synchronization Failure and Metastability.

Text Books

1. William J. Dally & John W. Poulton (2013); "Digital Systems Engineering", Cambridge University Press.

Reference Books

1. Howard Johnson & Martin Graham(1993), “High Speed Digital Design: A Handbook of Black Magic”, Prentice Hall PTR.
2. Masakazu Shoji(1996), “High Speed Digital Circuits”, Addison Wesley Publishing Company,
3. Jan M, Rabaey (2003), et all; “Digital Integrated Circuits: A Design Perspective” , Second Edition,

15ECVE1006/4

SYSTEM ON CHIP

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand the knowledge of the basic elements in a system: processor, memory, and interconnect
2. Understand issues in customizing and configuring designs.
3. Understand of the memory organization and interfacing issues**.**

UNIT I

Introduction to the System Approach - System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT II

Memory Design for SOC - Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT III

Interconnect Customization and Configuration - Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT IV

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books

1. Michael J Flynn, Wayne Luk (2011), "Computer System Design: System On Chip", Wiley India .

Reference Books

1. Steve Furber (2000), "ARM System on Chip Architecture", 2nd ed., Addison Wesley Professional.
2. Prakash Rashinkar, Peter Paterson and Leena Singh L. (2001), "System on Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers.
3. Ricardo Reis (2004), "Design of System on a Chip: Devices and Components" 1st ed., Springer.

15ECVE1051

VLSI DESIGN LAB

Lecture :	-	**Practical:**	3 Hrs/ Week	**Internal Assessment:**	40
Credits :	2			**Final Examination:**	60

Course Outcomes:

At the end of the course student will be able to

1. Get acquainted with programmable logic design flow.
2. Implement designed digital circuits using FPGA and CPLD devices.

List of Experiments

Task #1 Design and Synthesis of a RISC Stored-Program Machine

i. RISC SPM: ALU
ii. RISC SPM: Controller
iii. RISC SPM: Instruction Set
iv. RISC SPM: Controller Design
v. RISC SPM: Program Execution

Task #2 Design of communication and signal processing sub modules.

1. Design of 8-bit LFSR
2. Design of 4 bit Multiply and Accumulate unit
3. Design of A Hardware Multiplier
4. Design of Filter
5. Design an Huffman coder
6. Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.
7. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
8. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

Task #4 Design a coin operated public Telephone unit using Mealy FSM model with following operations

i. The calling process is initiated by lifting the receiver.
ii. Insert 1 Rupee Coin to make a call.
iii. If line is busy, placing the receiver on hook should return a coin
iv. If line is through, the call is allowed for 60 seconds at the 45th second prompt another 1 Rupee coin to be inserted, to continue the call.
v. If user doesn't insert the coin within 60 seconds the call should be terminated.

vi. The system is ready to accept new call request when the receiver is placed on the hook.

vii. The FSM goes 'out of order' state when there is a Line Fault.

15ECVE1052

EMBEDDED SYSTEM LAB

Lecture :	-	**Practical:**	3 Hrs/ Week	**Internal Assessment:**	40
Credits :	2			**Final Examination:**	60

Course Outcomes:

1. Design and execute the different concepts for embedded system using ARM processor

I. Experiments using ARM-:

1. Study of ARM processor kit
2. Simulation of arithmetic operation on ARM in assembly
3. Simulation of soft delay in assembly
4. Realization of input and output port in ASM
5. Simple led blinking with variable speed in ASM and in 'C'
6. Seven segment led display interface in 'C' and using ASM delay
7. Displaying alpha numeric characters in 2x16 lcd display
8. Converting Hexa decimal to Decimal and display in lcd display
9. Accessing internal ADC of the ARM processor and to display in lcd
10. Realizing timer peripheral in ARM by polling method and by interrupt driven method
11. Serial transmission and reception by polling method and by interrupt method

Lab Requirements:

Software:

(i) Keil IDE or Eclipse IDE for C and C++.
(ii) LINUX Environment for the compilation using Keil or Eclipse IDE.

Hardware:

(i) The development kits of ARM-7 or ARM-9 Developer Kits.

(ii) Serial Cables, Network Cables and recommended power supply for the board.

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15ECVE2001

LOW POWER VLSI DESIGN

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Apply different circuit techniques to manage the leakage currents
2. Comprehend existing low power adder and multiplier architectures
3. Understand the architectural and circuit level techniques for attaining low power consumption

UNIT I

Low power CMOS VLSI design - Introduction, sources of power dissipation, static power dissipation, active power dissipation.

Circuit techniques for low power design - Introduction, designing for low-power, circuit techniques for leakage power reduction.

UNIT II

Low voltage low power adders - Introduction, standard adder cells, CMOS adder's architectures, low voltage low power design techniques, current mode adders.

Low voltage low power multipliers - Introduction, overview of multiplication, types of multiplier architectures, braun multiplier, baugh-wooley multiplier, booth multiplier, wallance tree multiplier.

UNIT III

Low voltage low power static RAM - Basics of SRAM, memory cell, precharge and equalization circuit, decoder, address transition detection, sense amplifier, output latch, low power SRAM technologies.

Low voltage low power dynamic RAM - Types of DRAM, basics of DRAM, self refresh circuit, half voltage generator, voltage down converter, future trends and developments of DRAM.

UNIT IV

Low- Voltage Low Power Read-Only Memories - introduction, types of ROM, basics physics of floating gate nonvolatile devices, floating gate memories, basics of ROM, low power ROM Technology.

Text Books

1. Kiat Seng Yeo, Kaushik Roy (2005),"Low Voltage, Low Power VLSI Subsystems", TATA McGraw-Hil.

Reference Books

1. Yeo Rofail,Gohl (2002)," CMOS/BiCMOS ULSI Low Voltage, Low Power", Pearson Education Asia 1st Indian reprint.
2. J.Rabaey (1996), "Digital Integrated circuits: a Design Perspective", PHI.

15ECVE2002

ANALOG AND MIXED SIGNAL DESIGN

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Design single stage amplifiers and op-amp amplifiers
2. Analyze feedback amplifiers and oscillators.
3. Analyze the analog-digital converters and Comparators.

UNIT I

Single Stage Amplifiers and Current Mirrors - Common source, common gate and source follower stages- Cascode and folded cascode structures- Frequency response, MOS current mirrors-sources.

UNIT II

MOS Differential Amplifiers and Operational Amplifiers - Single ended and differential operation, Basic differential pair, Common mode response, Frequency response- CMOS operational amplifiers - One-stage op-amps and two stage op-amps

UNIT III

Feedback Amplifiers - General considerations, Feedback topologies

Oscillators and PLLs – General Considerations, Ring oscillators, LC oscillators, Voltage controlled oscillators, Basics of PLLs.

UNIT IV

Switched-Capacitor circuits – Sampling switches, Switched-Capacitor amplifiers, Switched-Capacitor integrator

Comparators and Analog-Digital converters – Two stage, Open-loop comparators, Parallel digital-analog converters.

Text Books

1. Behzad Razavi (2002), 'Design of Analog CMOS Integrated Circuits' Tata-Mc GrawHill.
2. Philip Allen & Douglas Holberg (2002), "CMOS Analog Circuit Design", Oxford University Press.

Reference Books

1. David A Johns & Ken Martin (2001), "Analog Integrated Circuit Design" John Wiley and Sons.

15ECVE2003

EMBEDDED DEVICE DRIVERS

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes:

Upon the completion of this course, students will be able to

1. Understands the Device Drivers need and loadable modules
2. Learn the debugging techniques and Advanced char driver operations
3. Understand fundamentals of hardware interface with kernel
4. Use and get acquaint to interrupt handling and kernel data types

UNIT I

An Introduction to Device Drivers - The Role of the Device Driver, Splitting the Kernel, Classes of Devices and Modules, Security Issues, Version Numbering

Building and Running Modules - Setting Up Your Test System, The Hello World Module, Kernel Modules Versus Applications, Compiling and Loading, The Kernel Symbol Table, Preliminaries, Initialization and Shutdown, Module Parameters, Doing It in User Space

Char Drivers - The Design of scull, Major and Minor Numbers, Some Important Data Structures, Char Device Registration, open and release, scull's Memory Usage, read and write, Playing with the New Devices.

UNIT II

Debugging Techniques - Debugging Support in the Kernel, Debugging by Printing, Debugging by Querying, Debugging by Watching, Debugging System Faults, Debuggers and Related Tools.

Concurrency and Race Conditions - Pitfalls in scull, Concurrency and Its Management, Semaphores and Mutexes, Completions, Spinlocks, Locking Traps, Alternatives to Locking

Advanced Char Driver Operations - octl, Blocking I/O, poll and select, Asynchronous Notification, Seeking a Device, Access Control on a Device File.

UNIT III

Time, Delays, and Deferred Work - Measuring Time Lapses, Knowing the Current Time, Delaying Execution, Kernel Timers, Tasklets, Workqueues

Allocating Memory - The Real Story of kmalloc, Lookaside Caches, get_free_page and Friends, vmalloc and Friends, Per-CPU Variables, Obtaining Large Buffers

Communicating with Hardware - I/O Ports and I/O Memory, Using I/O Ports, An I/O Port Example, Using I/O Memory.

UNIT IV

Interrupt Handling - Preparing the Parallel Port, Installing an Interrupt Handler, Implementing a Handler, Top and Bottom Halves, Interrupt Sharing, Interrupt-Driven I/O

Data Types in the Kernel - Use of Standard C Types, Assigning an Explicit Size to Data Items, Interface-Specific Types, Other Portability Issues, Linked Lists.

Text Books

1. Jonathan Corbet, Alessandro Rubini, and Greg Kroah-Hartman (2005), "Linux Device Drivers" O'Reilly Third Edition

Reference Books

1. Robert Love, "Linux Kernel Development", 3rd Edition, Addison-Wesley Professiona.
2. Sreekrishnan Venkateswaran, "Essential Linux Device Drivers", Prentice Hall

15ECVE2004

REAL TIME OPERATING SYSTEMS

Lecture :	4 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	4			**Final Examination:**	60

Course Outcomes

Upon the completion of the course student will be able to

1. Illustrate real time programming concepts.
2. Apply RTOS functions to implement embedded applications
3. Understand fundamentals of design consideration for embedded applications

UNIT I

Introduction to Real-Time Operating Systems - Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS

Task- Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency

UNIT II

Semaphores - Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use

Message Queues - Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables

UNIT III

Exceptions and Interrupts - Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts

Timer and Timer Services - Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.

I/O Subsystems - I/O concepts, I/O subsystems

UNIT IV

Memory Management - Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking VS. Non-Blocking Memory Functions, Hardware Memory Management Units

Synchronization and Communication - Synchronization, Communication, Resource Synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns,

Common Design Problems - Resource Classification, Deadlocks, Priority Inversion.

Text Books

1. Qing Li, Caroline Yao (2003), "Real-Time Concepts for Embedded Systems", CMP Books.

Reference Books

1. Albert Cheng, (2002), "Real-Time Systems: Scheduling, Analysis and Verification", Wiley Interscience.
2. Hermann Kopetz, (1997), "Real-Time Systems: Design Principles for Distributed Embedded Applications", Kluwer.
3. Insup Lee, Joseph Leung, and Sang Son, (2008) "Handbook of Real-Time Systems" Chapman and Hall.
4. Krishna and Kang G Shin, (2001), "Real-Time Systems", McGraw Hill.

15ECVE2005/1

TESTING AND TESTABLITY

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes

Upon the completion of the course student will be able to

1. Collapse the available faults in the system and use suitable simulation technique for testing
2. Test SSFs, Bridging faults in combinational and sequential circuits
3. Understand generation of test pattern in BIST and Analog testing complexity
4. Perform test response compression and analyze test complexity

UNIT I

Fault Modeling - Logical Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Single and Multiple Stuck-Fault Model.

Fault Simulation - General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT II

Testing For Single Stuck Faults – ATG for SSFs in combinational circuits- fault oriented ATG, Fault independant ATG, Random test generation, ATG for SSFs in sequential circuits- TG using iterative array models, Simulation based TG.

Testing For Bridging Faults – The Bridging Fault Model, Detection of Non-Feedback Bridging Faults, Detection of Feedback Bridging Faults, Bridging Fault Simulation.

UNIT III

Design For Testability - Testability, Adhoc Design for Testability Techniques, Controllability and Observability by Means of Scan Registers, Generic Scan Based Design**.**

Compression Techniques - General Aspects of Compression Techniques, Ones-Count Compression, Transition-Count Compression, Parity-Check Compression, Syndrome Testing, Signature Analysis.

UNIT IV

Built-In Self Test - Test Pattern Generation for BIST, Generic Off-Line BIST Architectures.

Introduction to Analog Testing - Analog signal test, Analog testing difficulties, Analog fault models, Levels of abstraction, Types of analog testing, DC fault simulation of non linear circuits, Linear analog circuit AC fault simulation.

Text Books

1. M. Abramovici, M.A. Breuer and A.D. Friedman (1996), “Digital Systems and Testable Design", Jaico Publishing House.

Reference Books

1. Parag K Lala (2002), “Digital Circuit Testing and Testability”, Achedamic Press.
2. M.L. Bushnell and V.D. Agrawal (2002), "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers.
3. A.L. Crouch (2002), "Design for Test for Digital IC's and Embedded Core Systems", Prentice Hall International.

15ECVE2005/2

EMBEDDED SYSTEM DESIGN

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand the general process of embedded system development
2. Interface to peripherals, knowledge of typical interfacing standards.
3. Develop an extensive insight into industrial applications and requirements.
4. Understand the multiple process operating environment and use standard system call interfaces to monitor and control processes

UNIT I

Introduction - An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT II

Embedded Software - Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.

Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

UNIT III

Embedded System Design, Development, Implementation and Testing - Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design.

Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT IV

Embedded System Design-Case Studies - Case studies- Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processor architectures should be taken into consideration while designing an Embedded System.

Text Books

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.

Reference Books

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

15ECVE2005/3

REAL TIME SYSTEMS

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon completion of the course students will be able to

1. Understands the RTOS loadable modules
2. Learn the debugging techniques
3. Understand fundamentals of hardware interface with kernel
4. Use and get acquaint to embedded application development

UNIT I

Categories of Embedded systems, Hardware architecture, Software architecture, Application software, Communication software, process of generating executable image, development/testing tools. GNU development tools, bit manipulation using C, memory management, timing of programs, productivity tools, code optimization.

UNIT II

Types of hardware platforms, 89C51 micro-controller development board, AVR micro-controller development board, need for communication interfaces, RS232/UART, RS422/RS485, USB, Infrared, Ethernet, IEEE802.11, and Bluetooth.

UNIT III

Off-the shelf OS, Embedded OS, RTOS, Handheld OS, OS software, Target image creation for windows XP embedded, Porting RTOS on a micro-controller based development board, Overview of Linux, Shell programming, System programming, Overview of RT Linux, Core RT Linux, API.

UNIT IV

Program to display a message periodically, development of navigation system, development environment, GPS receiver packet format, implementation, executing the program, development of protocol converter, design, implementation and testing, embedded database application, development environment, design, implementation, executing the program, DSP based embedded systems, an Overview of DSP, applications of DSP, Digital signal processor Architecture, DSP-based embedded system design process.

Text Books

1. Dr. K.V.K.K. Prasad: “Embedded/Real-Time Systems” Dream Tech Publications, Black pad book.

Reference Books

1. Labrosse, “Embedding system building blocks “, CMP publishers.
2. Rob Williams,” Real time Systems Development”, Butterworth Heinemann Publications.
3. Rajkamal: “Embedded Systems-Architecture, Programming and Design”, Tata McGraw Hill Publications, Second Edition, 2008.

15ECVE2005/4

PHYSICAL DESIGN AUTOMATION

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Comprehend the working of physical design flow.
2. Formulate CAD design using algorithmic paradigms
3. Understand design and automation of the FPGA's and MCM's.

UNIT I

VLSI Physical Design Automation - VLSI Design Cycle , Physical Design Cycle, New Trends, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

Fabrication Process and Its Impact - Fabrication Materials, Fabrication of VLSI Circuits, Design Rules, Layout of the Basic Design, Scaling Methods, Status of Fabrication Process, Issues Related to Fabrication Process, Future of Fabrication Process, Tools and Process Development.

UNIT II

Data Structures and Basic Algorithms - Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical Design.

UNIT III

Partitioning - Introduction to Partitioning, Problem Formulation, Classification of Partitioning Algorithm, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithm, Performance Drive Partitioning.

Floorplanning and Placement - Floorplanning, Chip Planning, Pin Assignment, Integrated Approach, Placement.

UNIT IV

Routing and Automation of FPGA's and MCM's - Global Routing, Detailed Routing, Clock Routing, Power and Ground Routing, Compaction, Physical Design Automation of the FPGA's and MCM's.

Text Books

1. Naveed A. Sherwani (1999), "Algorithms for VLSI Physical Design Automation", Third Edition, Kluwer Academic Publications.

Reference Books

1. S.H.Gerez (1998), "Algorithms for VLSI Design Automation", Wiley Publication.
2. Sadiq M. Sait and Habib Youssef (1999), "VLSI Physical Design Automation: Theory and Practice" by World Scienti Publishers, Singapore/Ne -Jersey, USA. (Also published by McGraw-Hill Book Co., Europe, December 1995).

15ECVE2006/1

HARDWARE SOFTWARE CO-DESIGN

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand architectural languages and co-synthesis algorithms for co-design.
2. Understand prototyping and emulation systems and target architectures.
3. Apply compilation tools and techniques for embedded processor architectures.

UNIT I

Co-Design issues - Co-Design Models, Architectures, Languages, A Generic Co-Design Methodology.

Co-Synthesis Algorithms - Hardware Software Synthesis Algorithms: Hardware – Software Partitioning Distributed System Co-Synthesis.

UNIT II

Prototyping and Emulation - Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping Architecture Specialization Techniques, System Communication Infrastructure

Target Architectures - Architecture Specialization Techniques, System Communication Infrastructure, Target Architecture and Application System classes, Architecture for Control Dominated Systems (8051-Architectures for High performance control), Architecture for Data Dominated Systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures - Modern Embedded Architectures, Embedded Software Development Needs, Compilation Technologies Practical Consideration in a Compiler Development Environment.

Design Specification and Verification - Design, Co-Design, The Co-Design Computational Model, Concurrency Coordinating Concurrent Computations, Interfacing Components, Design Verification, Implementation Verification, Verification Tools, Interface Verification

UNIT IV

Languages for System – Level Specification and Design-I - System – Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages,

Languages for System – Level Specification and Design-II - Heterogeneous Specifications and Multi-Language Co-Simulation the Cosyma System and Lycos System.

Text Books

1. Jorgen Staunstrup. (2009), “Hardware / Software Co-Design Principles and Practice” Wayne Wolf Springer.

Reference Books

1. Jean-Michel Berge (1997), “Hardware/Software Co-Design and Co- Verification”, Kluwer Publications.

15ECVE2006/2

EMBEDDED NETWORKING

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon completion of the course the students will be able to

1. Understand the fundamentals of embedded systems programming, real-time operating systems
2. Explore newly established standards for embedded systems and ubiquitous computing
3. Analyse and specify requirements for network technologies based on example application scenarios.
4. Evaluate the performance of communications protocols used in a networked embedded system

UNIT I

Advanced Communication principles - Embedded Networking: Introduction – Serial/Parallel Communication – Wireless communication, Layering -Serial Protocols – Parallel protocols - Wireless protocols.

UNIT II

USB and CAN Bus - USB bus-Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III

Ethernet Basics - Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

Unit IV

Embedded Ethernet - Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

Text Books

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.

2. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
3. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003

Reference Books

1. Rajkamal, ―Embedded Systems Architecture, Programming and Design‖, TATA McGraw-Hill, First reprint Oct. 2003.

15ECVE2006/3

VLSI SIGNAL PROCESSING

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon the completion of this course, students will be able to

1. Apply the concepts of pipelining, parallel processing, Retiming, Folding and unfolding to optimize digital signal processing architectures
2. Analyze data flow in systolic architectures.
3. Minimize the computational complexity using fast convolution algorithms.
4. Analyze pipelining and parallel processing of IIR filters

UNIT I

Introduction to DSP - Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing - Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

UNIT II

Retiming - Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

Folding - Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of Multirate systems

Unfolding - Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT III

Systolic Architecture Design - Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

Fast Convolution - Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT IV

Pipelined and Parallel Recursive and Adaptive Filters – Introduction - Pipeline Interleaving in Digital Filters, Pipelining in 1st-Order IIR Digital Filters, Pipelining in Higher-Order IIR Digital Filters, Parallel processing for IIR Filters, Combined Pipelining and Parallel Processing for IIR Filters.

Text Books

1. Keshab K. Parthi. (1998), "VLSI Digital Signal Processing- System Design and Implementation", Wiley Inter Science.

Reference Books

1. Jose E. France, Yannis Tsividis. (1994) "Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing", Prentice Hall.
2. Medisetti V. K . (1995), "VLSI Digital Signal Processing", IEEE Press (NY), USA.

15ECVE2006/4

PERL SCRIPTING LANGUAGE

Lecture :	3 Hrs/ Week	**Practical:**	-	**Internal Assessment:**	40
Credits :	3			**Final Examination:**	60

Course Outcomes:

Upon Completion of the course the students will be able to

1. understand the PERL script constructs at every level of abstraction
2. understand the data structures in PERL script
3. apply PERL script to compile, execute and debug the code

UNIT I

An Overview of Perl- Natural and artificial languages, variable syntax, verbs, an average example, File handles, Operators- Some Binary Arithmetic Operators, String Operators Assignment Operators, Unary Arithmetic Operators, Logical Operators, Some Numeric and String Comparison Operators, Some File Test Operators, Regular Expressions - Quantifiers, Minimal Matching, Nailing Things Down, Back references, List Processing, Unary & Binary Operators.

UNIT II

Statements and Declarations - Simple Statements, Compound Statements, if and unless Statements, The given Statement, Loop Statements, The goto Operator, Paleolithic Perl Case Structures, The Ellipsis Statement, Global Declarations, Scoped Declarations, Pragmas.

Pattern Matching - Pattern Matching Operators, Metacharacters and Metasymbols, Character Classes, Quantifiers, Positions, Grouping and Capturing, Alternation, Staying in Control, Fancy Patterns.

Subroutines - Syntax, Semantics, Passing References, Prototypes, Subroutine Attributes.

UNIT III

Data Structures - Arrays of Arrays, Hashes of Arrays, Arrays of Hashes, Hashes of Hashes, Hashes of Functions, More Elaborate Records, Saving Data Structures.

Packages - Symbol Tables, Qualified Names, The Default Package, Changing the Package, Autoloading.

Modules - Loading Modules, Unloading Modules, Creating Modules, Overriding Built-in Functions.

Objects - Brief Refresher on Object-Oriented Lingo, Perl's Object System, Method Invocation, Object Construction, Class Inheritance, Instance Destructors, Managing Instance Data, Managing Class Data, The Moose in the Room.

Tied Variables - Tying Scalars, Tying Arrays, Tying Hashes, Tying Filehandles

UNIT IV

Interprocess Communication - Signals, Files, Pipes, System V IPC, Sockets.

Compiling - The Life Cycle of a Perl Program, Compiling Your Code, Executing Your Code, Compiler Backends, Code Generators, Code Development Tools.

The Command-Line Interface - Command Processing, Environment Variables.

The Perl Debugger - Debugger Commands, Debugger Customization, Unattended Execution, Debugger Support, Profiling Perl.

Text Books

1. Larry Wall, Tom Christiansen, John Orwant, (2012) "Programming PERL", 4th Edn., Oreilly Publications.

Reference Books

1. Randal L, Schwartz Tom Phoenix, (2000) "Learning PERL",3rd Edn., Oreilly Publications.
2. Tom Christiansen, Nathan Torkington, (2000) "PERL Cookbook", 3rd Edn, Oreilly Publications.

15ECVE2051

ANALOG & DIGITAL IC LAB

Lecture :	-	**Practical:**	3 Hrs/ Week	**Internal Assessment:**	40
Credits :	2			**Final Examination:**	60

Course Outcomes:

Upon Completion of the course the students will be able to

1. design and analyze digital, analog MOS circuits

List of Experiments

Design the following circuits with given specifications, completing the design flow mentioned below:

a. Design and perform the following analysis as per the requirement
   i. DC
   ii. Transient
   iii. Op
   iv. AC
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design
e. Verify & Optimize for Time, Power and Area to the given constraint

1. Common source amplifier
2. Common gate amplifier
3. Common drain amplifier
4. Common source amplifier with negative feed back
5. Current mirror
6. Differential amplifier
7. Inverter
8. Nand, Nor gate
9. 4x1 Mux using pass transistors/ transmission gates
10. Dynamic logic gates
11. SRAM memory cell
12. Ring oscillator

Text Books

1. J.Rabaey (1996), “Digital Integrated circuits: a Design Perspective”, PHI
2. Behzad Razavi (2002), ‘Design of Analog CMOS Integrated Circuits’ Tata-Mc GrawHill.

15ECVE2052

EMBEDDED SYSTEM DESIGN LAB

Lecture :	-	**Practical:**	3 Hrs/ Week	**Internal Assessment:**	40
Credits :	2			**Final Examination:**	60

Course Outcomes:

Upon Completion of the course the students will be able to

1. Design and execute the different RTOS concepts for embedded system design
2. Developing the RTOS application on ARM Processor

I. Experiments using ARM with RTOS:

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.
9. Implement the interfacing of display with the ARM- CORTEX processor.
10. Interface ADC and DAC ports with the Input and Output sensitive devices.
11. Simulate the temperature DATA Logger with the SERIAL communication with PC.
12. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(iii) The development kits of ARM Developer Kits.

(iv) Serial Cables, Network Cables and recommended power supply for the board.

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